Consortium For On-Board Optics

Multimode Waveguide Interconnect System Design for Photonic Circuit Integration

White Paper

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Abstract and Author Contacts

We propose a novel interconnection architecture, 'MMWG (multimode waveguide) system', in order to address the most recent issues on system power consumption and bandwidth limitation for Data Center application.

MMWG system is defined to replace copper trace with optical multimode waveguide embedded in PCB layers for high-speed signal path in order to increase overall power efficiency and traffic bandwidth. We have simulated the eye diagram performance for 0.25 and 0.5 meters length of polymer MMWG with misaligned connector interfaces.

It is observed that the modal dispersion is dependent on MMWG length, while it is independent to misalignment between MMWG and connector. Overall, the power efficiency of MMWG increases significantly even with the addition of newly defined optical interface called MA (MMWG Adaptor) consuming less than ~0.35pJ/bit regardless of the MMWG length inside the box as a low powered hypothetical LTI interface. Eye-diagram of 100Gbps signal shows clear open eye through linear electrical filter. Higher speed eye-diagram was also simulated for further discussion. This paper was originally published at the DesignCon Conference.

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1. Introduction

1.1 - Background and Challenges

As the information traffic increases in Data Centers, major standard activities for highspeed connectivity, such as IEEE 802.3 and OIF CEI, plan to put more efforts into technologies to increase the switching system bandwidth especially in the areas of SERDES and interconnection technology. It is known that as the signal speed increases, the quality of the signal becomes more impaired due to the limited channel bandwidth. This makes the interconnection system consume more power to compensate the impairments.

Such an increase of power can be explained by two major reasons:
(1) the insertion loss (IL) of PCB trace increases monotonically as a function of frequency, requiring more power to compensate the signal to the required level at the receiving end; and (2) higher speed digital signal requires more taps of digital equalizer, accordingly more power, to compensate a greater number of bits due to the increased bitrate.

These are the two main reasons for increased SERDES power consumption, although there are some mitigations through advanced silicon fabrication technologies (i.e., advanced node). Therefore, the increase of power consumption is an inevitable on-going trend. It becomes a formidable challenge for Data Center's operation, as well as equipment vendors.

It is very recent to realize that the industry faces the hard barrier in 'wall plug' power limitation for the given real-estate footprint, which becomes the primary motivation for the breakthrough technology called CPO (co-packaged optics) system shown in Figure 1.

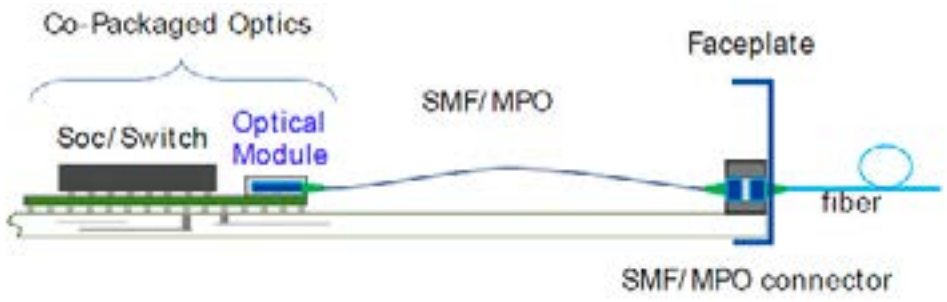


FIGURE 1 – Co-Packaged Optics adresses the Imminent Issue of Bandwidth and Power Consumption

While meeting the ever-increasing bandwidth requirement, CPO applies the power saving concept of bringing the optical module inside the box from the faceplate, where the conventional pluggable optics are present, thereby reducing the copper trace length, overall IL and the number of taps of digital equalizers. This innovative idea has been gaining momentum and consensus recently by the eco-system among the major standard bodies.

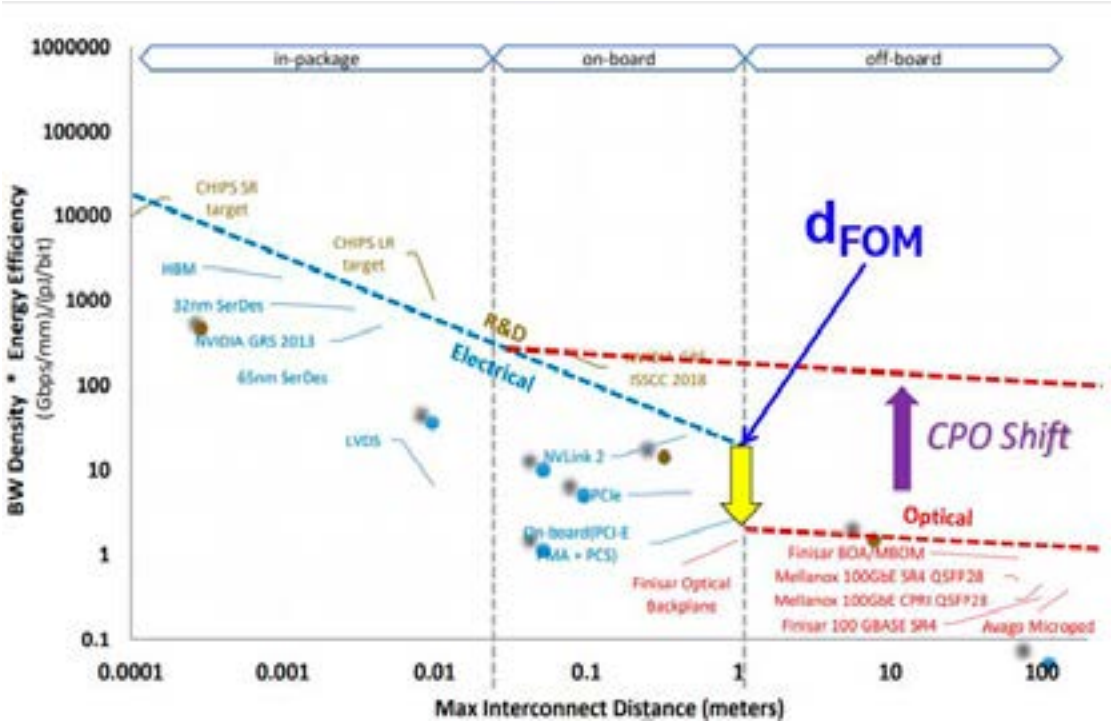


FIGURE 2 – FOM (Figure of Merit) For Co-Packaged Optics (FROM [1]) and dFOM (delta-FOM)

One recent contribution to IEEE 802.3 'Beyond 400G' study group shared the Figure of Merit (FOM) of CPO among other technologies as shown in Figure 2[1], where the FOM is defined as the product of the bandwidth density (Gbps/mm) and power efficiency (PE) in the unit of bit/pJ. The various SERDES technologies scattered on the chart shows a declining FOM trend as it moves from XSR (in-package) to VSR (on-board) (i.e., positive x direction) because of the two above mentioned reasons together with the physical size increase in their form factor from the CPO's optical module to the conventional pluggable optics.

Thus, one can expect the jump of FOM, noted as 'CPO Shift'[1]. In short, this jump is attributed to the reduction of both copper trace and package dimension. On the other hand, the FOM trend in conventional optical modules (lower-right dotted line) seems to be less optimized in terms of FOM, which shows a big gap of about 10 times less than electrical technologies at the faceplate location (around x=1m) denoted as dFOM.

The reason for this gap could be explained by the fact that the optical module has two entities in one package footprint responsible for driving both copper trace inward and optical fiber outward, which in general consumes much higher power. Moreover, the conventional optical module is located at the faceplate and physically constrained by RU (Rack Unit) and standardized optical connectors.

Therefore, the bandwidth density is limited by the faceplate of the box. However, the faceplate will not likely be removed because of its active function as a demarcation point and physical protective boundary. So, for CPO to be deployed in a system, a separate passive optical connector must be provided at the faceplate as shown in Figure 1.

This additional passive connection is not desirable, especially when multi-fiber connectors are used (e.g., MPO of 12 fibers) and the optical power budget of given (or standard) reach length is tight.

(1) Because of high loss for high fiber-count connectors, CPO optical engine faces some challenges to compensate such optical connector loss, which will bring us back to the ‘power issue’.

(2) Another challenge is that the big size of CPO modules obstructs air flow and adds extra thermal mass.

(3) Fiber handling during box-assembly is a potential human error source. Thus, even though CPO system brought about some consensus in the eco-system, there will be some foreseeable drawbacks of its architecture.

2. Architecture Proposal: Optical MM Waveguide Systems

2.1 - Proposed Application

Figure 3 shows the proposed system [2] of this paper, which uses printed optical waveguide (specifically multimode waveguide) inside the PCB layer for interconnection path between switch chip and optical module (or chip). This system increases the interconnection bandwidth and power efficiency (bit/pJ) and removes human error during the assembly process.

FIGURE 3A - Proposed Interconnection Scheme for Chip to Module (Chip) : NPO-like

FIGURE 3B - Proposed Interconnection Scheme for Chip to Module (Chip) : CPO-like

Figure 4 shows the state-of-the-art optical waveguide embedded in typical PCB (or Printed Optical Board).

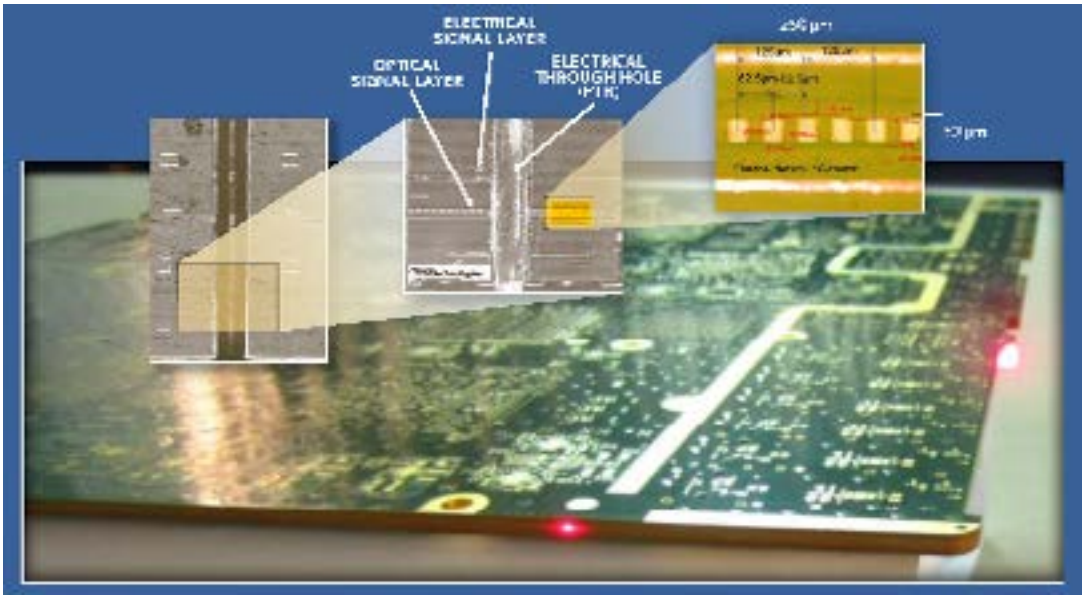


FIGURE 4 – Matured MMWG Technology Embedded in Multi-Layered PCB (by Courtesy of TTM Inc.)

In order to review the energy efficiency of the proposed system, we first compare the architectural design for a conventional system and a CPO system in Figure 5.

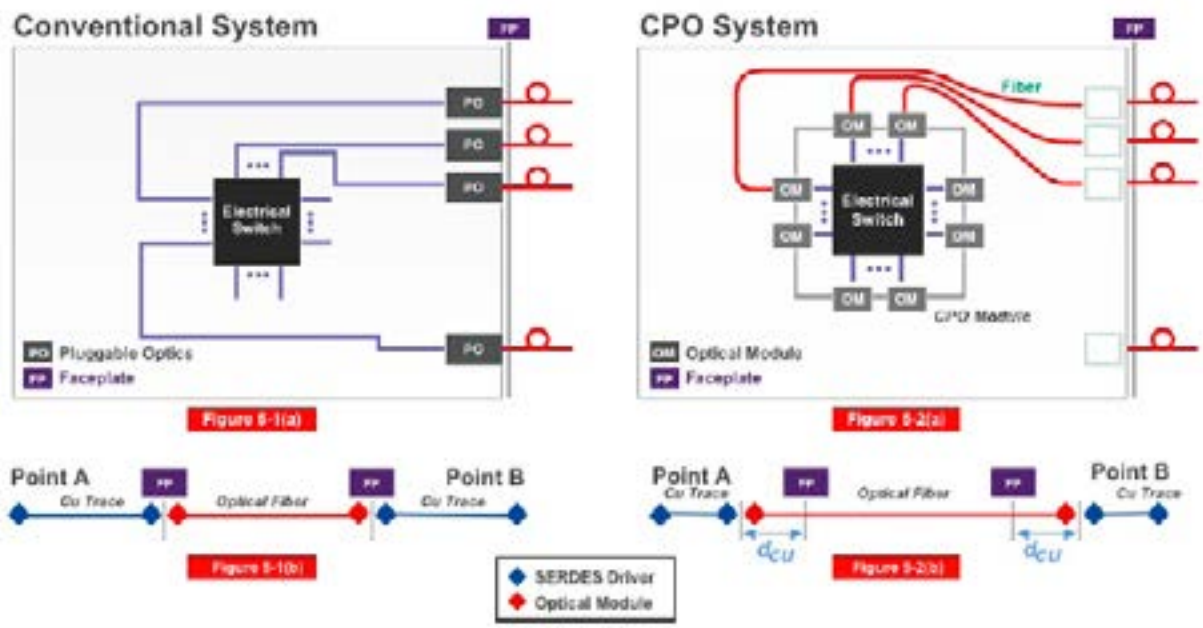


FIGURE 5 - Block Diagrams of a Conventional System and a CPO System (a) and Link Models (b)

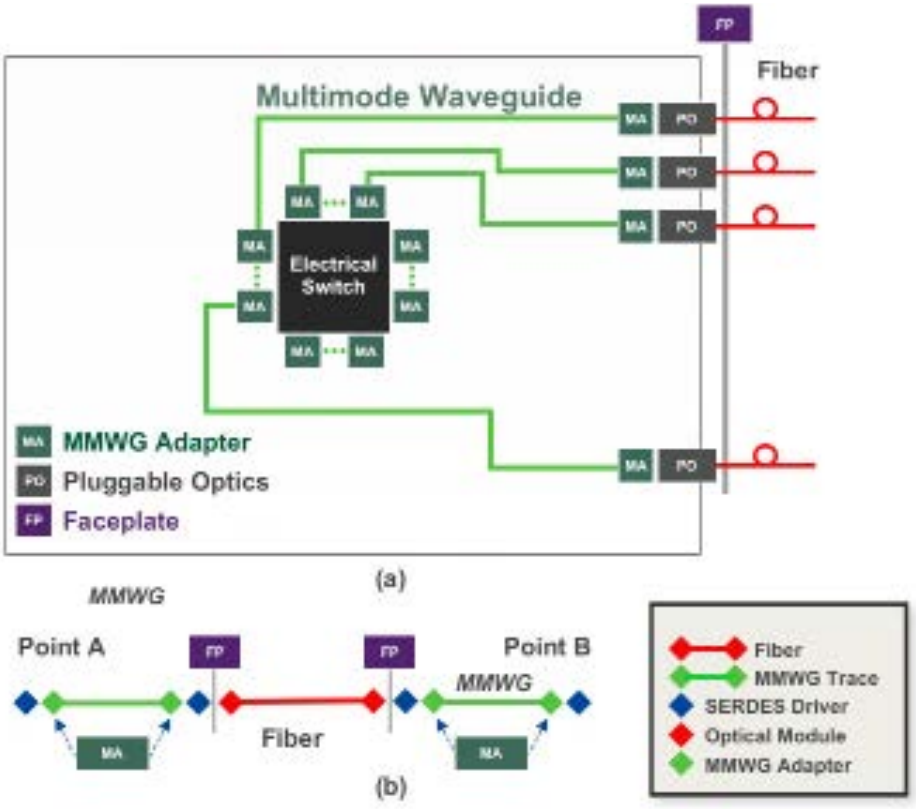


FIGURE 6 - Block Diagram (a) and and Abstract Link Model (b) For MMWG System

The link model of a conventional system (Figure 5-1(a) is shown in Figure 5-1(b) to elaborate the signal path. It starts from the SERDES 'Point A' [(depicted as) 1st diamond] of switch chip in the transmitter (TX), goes through the copper electrical trace and is terminated at the faceplate [2nd diamond at FP]. The faceplate serves as a demarcation point where the signal is relayed from the electrical input of the optical pluggable module [3rd diamond] to the long reach optical fiber for various reach options and finally terminated at the far end of the fiber link [4th diamond]. The transmission media is reverted back to copper trace at the electrical output of the optical pluggable module [4th-to-5th diamond] and finally terminated at 'Point B' of the RX chip [6th diamond].

On the other hand, a CPO (co-packaged optics) system shown in Figure 5-2(a) uses optical fiber to interconnect the CPO module (e.g., switch) and the faceplate, while the OM (optical module) is co-located with the switch chip inside the CPO module. The switch chip and OM are interconnected through a short copper trace (10dB max). Figure 5-2(b) shows the abstract link model of the CPO system, where the optical link is further intruded inside each box so that the length of copper trace is reduced ($-dl_{CU}$), whereby the amount of power, dl_{CU}*ES_{CU}, can be saved, where ES_{CU} is the slope of EPB (Energy Per Bit) per dB of IL as an equivalent length at Nyquist frequency.

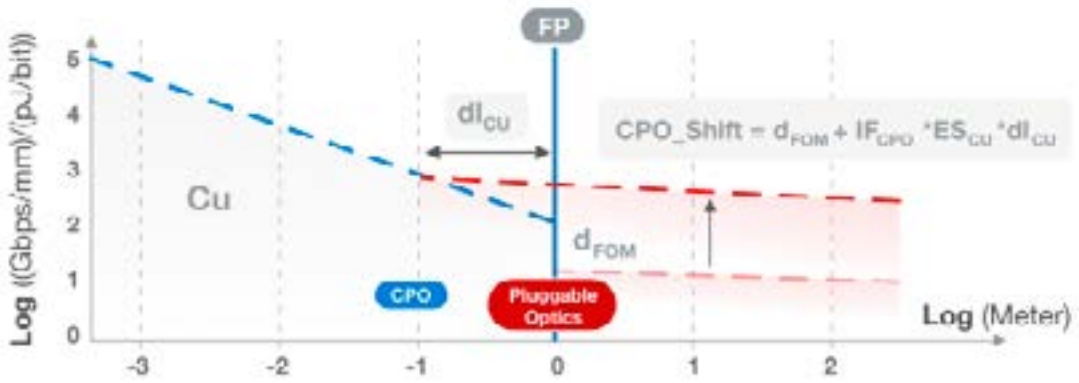


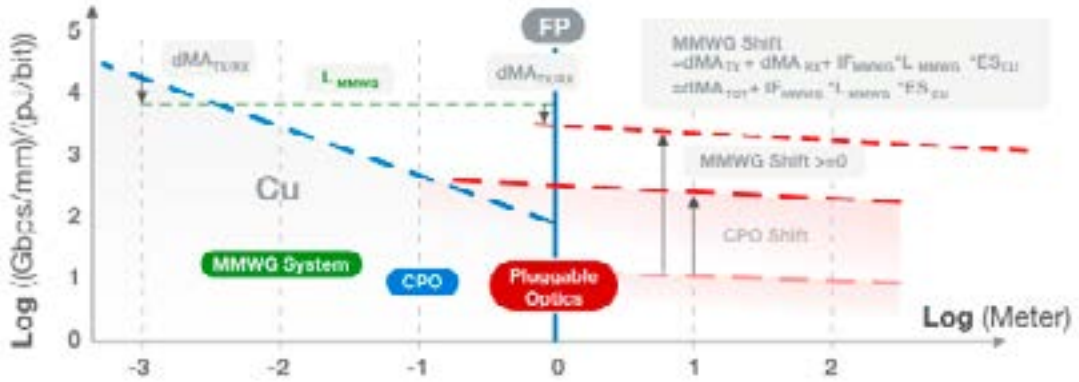
FIGURE 7 - FOM as a Function of Insertion Loss and Reduced Cu Trace (dCU)

This is further explained through the hypothetical FOM plot (Figure 7) of 'CPO_shift' (previously shown in Figure 2), where IF_{CPO} is the integration factor of CPO packaging. Thus, the CPO system ideally removes d_{FOM} and replaces copper trace (dl_{CU}) with fiber so that overall FOM gain could be achieved: CPO_Shift = d_{FOM} + IF_{CPO}*ES_{CU}*dl_{CU}. Note that currently the maximum optical reach for CPO is 2km (FR).

Similarly, Figure 6 shows (a) the block diagram and (b) the abstract link model of the proposed MMWG system. As mentioned above, the MMWG system is defined to replace the copper trace with the optical waveguide embedded in PCB and a newly defined thin interface called 'MMWG adaptor (MA)' at both ends of the optical trace (MMWG).

In order to get the power efficiency of MMWG system, MA is further explained in the link model shown in Figure 6(b). The electrical switch output buffer [1st diamond] drives the MA at the Tx [2nd diamond] to do e/o (electrical/optical) signal conversion and send the optical signal through the MMWG. The optical signal is terminated with o/e conversion at the input of MA at Rx [3rd diamond] right before the faceplate [4th diamond at FP], where the conventional optical pluggable module [5th diamond] takes the electrical signal from the output of the same MA at Rx [4th diamond] and converts it to an optical signal for the long reach fiber. The remaining path from the Rx side of the fiber is in the reverse order.

Thus, the MMWG link removes copper traces except for the electrical interface points at MAs, which add extra power consumption along with the new integration factor (IF_{MMWG}). However, since the MA should add minimal power consumption for signal conversion, it is defined to minimize the additional power, so that overall, it should still give a gain in power efficiency (PE).



IFmmwg = Integrating factor of multimode waveguide, Lmmwg = Length of multimode waveguide.

FIGURE 8 - FOM Requirement For MMWG System

Figure 8 explains this requirement of the MA in order to produce a positive 'MMWG shift' in FOM:

[MA Requirement] $|dMA_{TOT}| \leq L_{MMWG} * ES_{CU}$

where $dMA_{TOT} = dMA_{TX} + dMA_{RX}$ is FOM decrease by adding MA with the assumption of $IF_{MMWG} \geq IF_{CPO}$, which is a feasible condition when considering the shrinking dimension from a CPO system to an MMWG system. (The equality imposes the size requirement.) Note that the MMWG FOM line stays flat reflecting the fact that the optical path is non-dispersive for this short distance and form factor is negligible as the MMWG has no standard connectors inside the box.

For example, a typical polymer MMWG optical insertion loss of 0.05dB/cm for 850nm of light signal has been reported, yielding only 1.25dB for 10" of length, as opposed to 16dB for copper with equivalent length, which explains the flatness [3].

3. Power Efficiency For MMWG

In this section, we will review the viability of the requirement derived in the previous section [MA Requirement] through a practical exemplary application. First, in order to get ES_{CU}, we collected data points for average EPB (energy per bit) for 100G copper SERDES (through verbal communication with eco-system partners) per each subclass interconnection method described in the standards (IEEE 802.3 and OIF-CEI specifications) shown in Figure 9(a) and are plotted as a function of IL(dB), Figure 9(b), which shows.

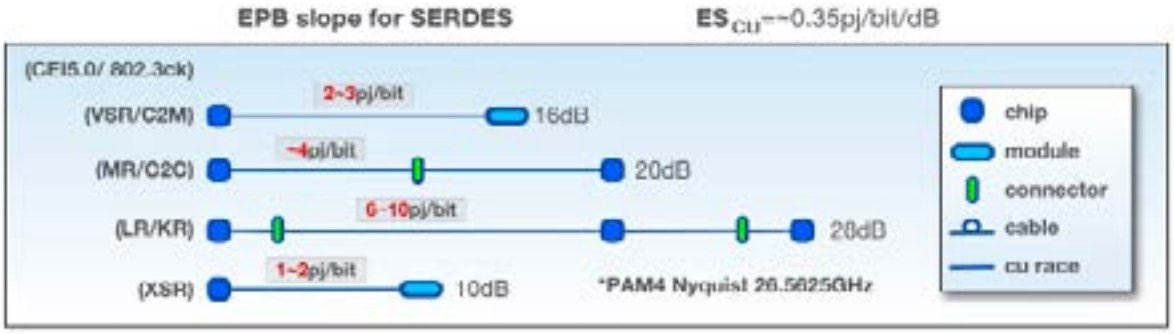


FIGURE 9a - FOM Requirement For MMWG System

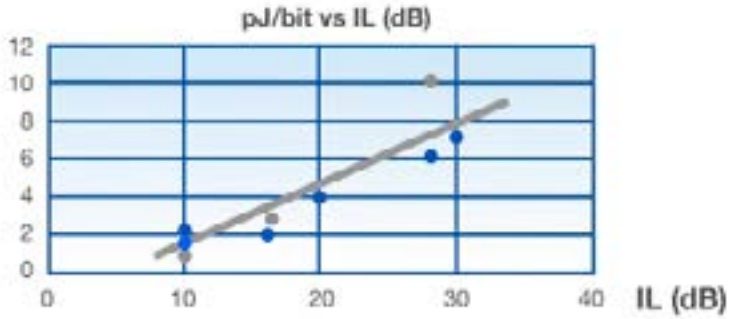


FIGURE 9b - SERDES EPB (Energy per Bit) vs IL

This can translate into 123W of power saving for a switching system of 100G port of the 128-radix by removal of 16dB copper trace of C2M (or VSR), while 77W of power saving for the same system with CPO by removal of 10dB copper trace (XSR). However, in order to get such power savings in an MMWG system, minimal power must be supplied for the MMWG adaptation. To get some insight about the amount of such additional power consumption, the function of the MA is described here in detail. Fundamentally, the MA should provide a simple 'transfer function' for a given electrical(/optical) signal from(/to) electrical to(/from) optical medium in LTI (linear time invariant) system: no re-timer and no re-shaper are assumed.

The simplicity of MA is the key for the minimal additional power requirement as mentioned earlier. In fact, at some standard bodies, there are on-going discussions of a similar topic called 'direct drive' option for Laser diode (LD) and Photo diode (PD) for CPO implementation. Thus, the ideal MMWG link is composed of a light source (Transconductance Amplifier + LD), short waveguide and light sink (PD + Transimpedance Amplifier) as shown in Figure 10.

FIGURE 10 - MMWG Link Model For Energy Per Bit (EPB) Calculations

The one-meter length limit of L_{MMWG} is presumably used suggesting a typical maximum electrical trace length in the box. The length of copper trace of IL_{MA}~0 inside MA block is to represent the case when MA is ideally integrated in a PIC (Photonic Integrated Circuit) monolithically. In the case that some minimal copper trace of for implementation is needed, it is possible to use such a short copper trace as long as the MA holds the LTI condition.

Let us consider a very simple, but ideal, model of an MMWG link surrounded by a standard electrical characteristic impedance, Z_0, to estimate the power efficiency, EPB (energy per bit) of the MMWG link. It is composed of LD (VCSEL 850nm), PD, optical connectors, and MMWG. A further assumption has been made that there is negligible chromatic or modal dispersion because of a short length of optical waveguide. Moderate optical IL is present from various roots, such as material loss, IL_{MAT} (dB/cm) including geometrical imperfections of the waveguide (e.g., surface roughness) and the coupling loss of all connectors, L_{CPL}(dB), at any possible interface. (However, modal dispersion will be discussed at the next section in detail which could be critical when the bitrate (BR) goes high enough.)

With these in mind, assuming Vin is the incoming signal amplitude (in volt) at the TCA (Transconductance Amplifier) of MA_{TX} (MA in Tx function) in Figure 10 from the electrical transmission line of Z_0, the received signal generates I_{TCA_AVG} by transconductance (gm) under the impedance matched condition, which is completely consumed by the heat and photon generation through the injection current of LD, I_{LD_AVG}, consumes power through the forward voltage of VCSEL, V_{LD_AVG}. Dividing this by BR gives the first EPB_{LD}. If the required I_{LD_AVG} is less than minimum I_{TCA_AVG}, that can be generated by $gm=1/Z_0$ (assuming impedance matched LD bias circuit), then ideally a TCA is not required nor extra power, which is the case in general.

On the other hand, the launched optical signal, after the total optical loss, IL_{TOTAL} (= IL_{MAT}*L_{MMWG} + L_{CPL}), is received at the PD which generates average photo current, I_{PD_AVG}, with bias voltage applied, V_{PD_BIAS}, that will finally produce EPB_{PD}. Then, the photocurrent I_{PD_AVG} is fed into TIA (transimpedance amp) with feedback impedance of tz (Ohm) which is determined by the dynamic range of I_{PD_AVG} = [I_{PD_MIN} , I_{PD_MAX}] for the desired output voltage, V_{OUT}, to drive the electrical transmission line with characteristic impedance, Z_0. V_{OUT} can be generated only by received I_{PD_AVG} or may need the extra external booster when I_{PD_AVG} is too small to drive V_{OUT}. As a summary, EPB equations derived from the above argument are,

[EQ1] EPB_{TCA}=0
[EQ2] EPB_{LD}= I_{LD_AVG} * V_{LD_AVG} /BR
[EQ3] EPB_{PD}= I_{PD_AVG} * V_{PD_BIAS} /BR, and
[EQ4] EPB_{TIA}= MAX($I_{PD\_AVG}^2$*(V_{OUT} / I_{PD_MIN} +Z_0)/BR, V_{OUT}^2/Z_0/BR).

Considering typical operational condition of MMWG link for 112Gbps using VSCEL and PIN-PD, with I_{LD_AVG} of 2~5mA, V_{LD_AVG} of 2~3V, I_{PD_AVG} of 0.1~2mA, V_{PD_BIAS} of 2~3V, and Z_0 of 100Ohm and with $V_{IN/OUT}$ of 400mVpp (nominal), we have

[EQ5] EPB_{TOT_MAX}= 352 fJ/bit (= 0+134+54+164)
[EQ6] EPB_{TOT_MIN}= 71fJ/bit (=0+54+3+16).

This result shows that the maximum additional power, 0.35pJ/bit, by the MA is considerably small that one can even get back by reducing copper trace of only 1.0 dB IL (= $EPB_{TOT'MAX}$ / ES_{CU}). This means whenever the MMWG is applied to replace the copper trace of more than 1.0 dB IL, the MMWG approach is effectively saving power, even when compared to the CPO architecture.

Reflecting this to the same system that we have discussed earlier (100G port system with the radix of 128 system), this additional EPB_{TOT_MAX} will add to the power consumption by 9W. Thus, overall, even with the addition of MAs, saves 114W (=123-9) by replacing VSR copper into MMWG and 68W (=77-9) by replacing XSR copper into MMWG system (MMWG+MAs).

4. Link Performance and Simulation

In this section, the performance of a MMWG link through eye diagram analysis is discussed. As mentioned earlier, multimode waveguides are adopted because of their mechanical alignment advantage. It is particularly important for automated PCB assembly processes in order to ensure the optical power stays within the budget of the link. Here we have used a typical MMWG cross-sectional size of 48umx48um embedded in layers of conventional PCB processes.

However, since the physical dimension of the waveguide is larger than its operational wavelength, the waveguide falls into the "multimodal" category. This means that there is more than one mode for signal transfer in the waveguide, which results in less channel bandwidth than single mode. Moreover, since high-speed active optical components have single mode interfaces in general, the optical interface of MA requires a mode conversion, which is a connector design challenge.

Here, we simulate the MMWG link in time domain to see if (1) this multimode dimension provides good enough bandwidth technology solution for Data Center applications and (2) any other modal noise might be created when the connector is misaligned with the MMWG by the lateral displacement, d_{MIS}.

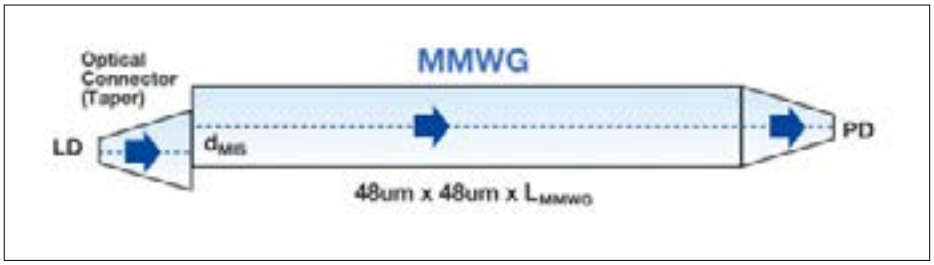


FIGURE 11 - Simulation Model For Misalignment Induced Model Dispersion

Figure 11 shows the simulation link model reflecting the above situation. The waveguide cross sectional dimension (48um x 48um) and material constants (RI core/clad = 1.57/1.544) from a typical optical PCB manufacturing process were used.

For simulation, we used a commercially available Eigenmode Expansion (EME) solver to get optical transfer function (S21.^2). As a quick performance test method to assess the modal dispersion, we simulated the FIR (Finite Impulse Response) for 0.25 meters and 0.5 meters of MMWG interconnection length as a function of d_{MIS}(um).

The field propagation profile of the waveguide of L_{MMWG} = 32mm with the misalignment d_{MIS} = 5um is shown in Figure 12 just to give some insight about how the light propagates inside the MMWG and converts back to single mode interface. It is noteworthy that although the MMWG physical dimension is in near ray optics regime (48um >> 0.85um), a wave optics characteristic still appears in the plot rather than showing straight optical lines of rays (zig-zag reflection patter). Thus, eigenmode based simulation was justified to be used so that it reflects the precise coherent transfer function of the MMWG system inside the e/o/e (electrical-optical-electrical) link.

Figure 13 shows the transfer function of MMWG as a function of length, L_{MMWG}, when d_{MIS} =10 um. Small but clear intensity fluctuations are observed due to the wave nature of coherent interference as expected. Even though the fluctuation is small (max 1.54dB), this may cause performance degradation of the link. A feedback circuit might be applied to maintain the desired constant electrical output signal such as automatic gain controller (AGC), which would not be an attractive solution since it increases power consumption.

However, one could consider (1) optimizing the dimensional parameters of waveguide itself to suppress such fluctuations in purely optical domain and/or (2) modifying the electric buffer so that the optimized threshold level absorbs such fluctuations with specified margin with the aid of non-linear passive electrical circuit (e.g.,-clamping diode).

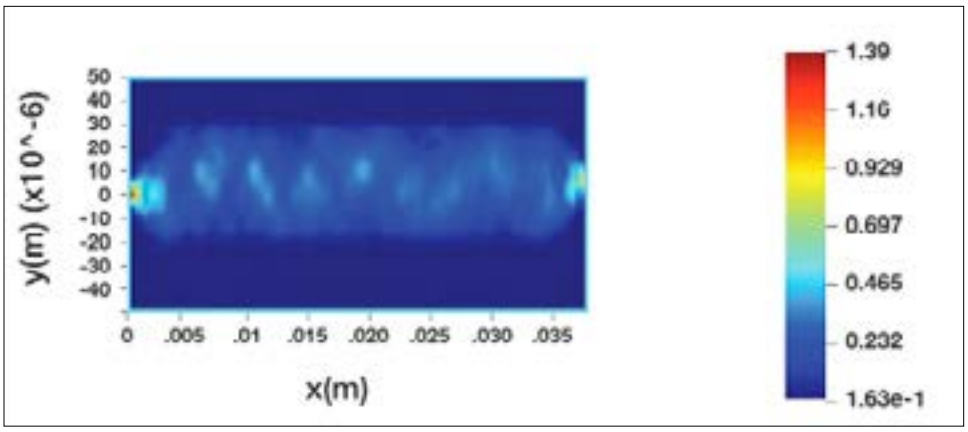


FIGURE 12 - Field Profile Simulation For L_{MMWG}=320um and d_{MIS}=5um

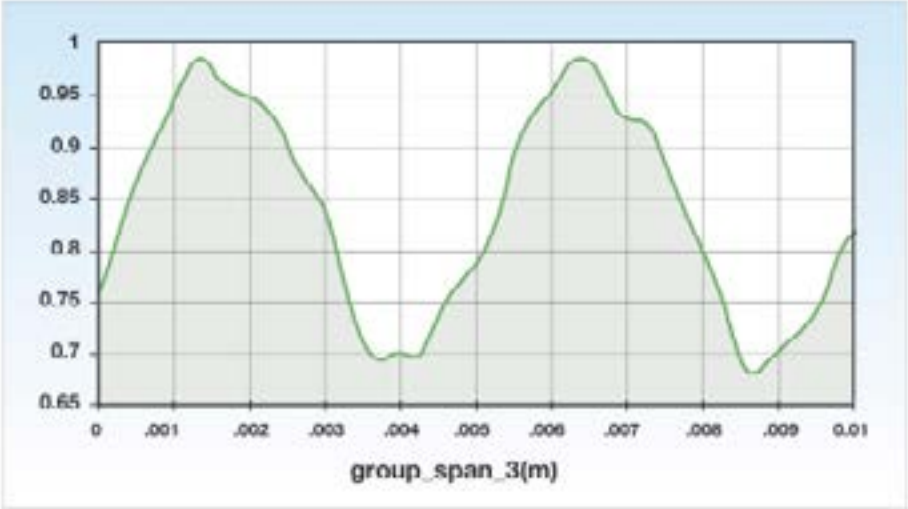


FIGURE 13 - Fluctuation of Transfer Function vs MMWG Length

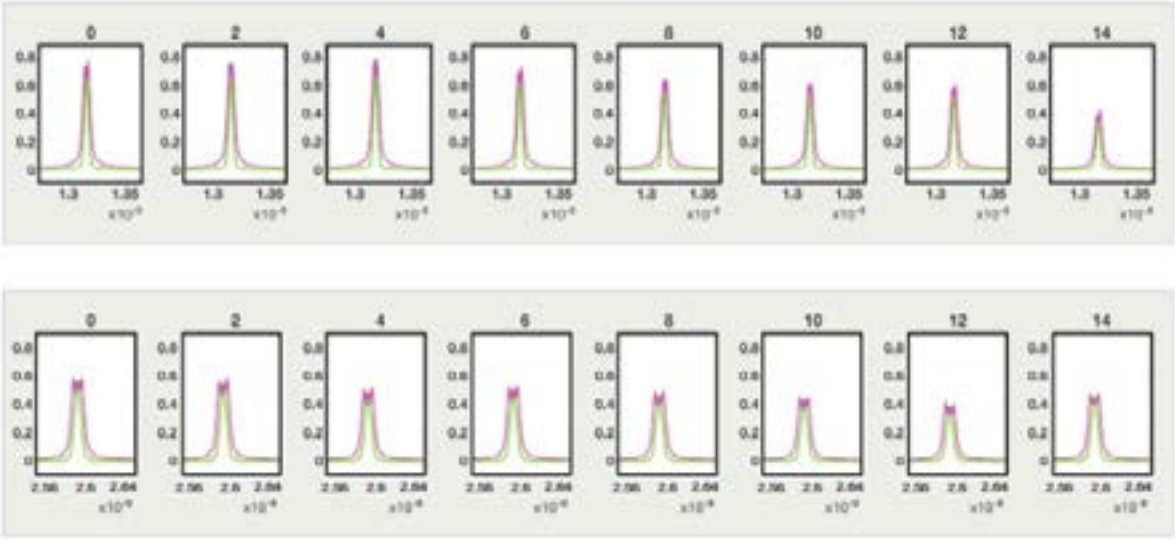


FIGURE 14 - FIR Simulation (a) L_{MMWG}=0.25 Meter (b) L_{MMWG}=0.5 Meter with Gaussian Filter (Green)

Figure 14 shows the finite impulse response with and without gaussian filter of the sigma of 100GHz (green and magenta) when L_{MMWG} = 0.25 meters and 0.5 meters while the misalignment amount, d_{MIS}, varies from 0 to 14 um (in 2um steps), where y-axis is optical intensity (arbitrary unit). As shown in the figure, the optical power decreases as the misalignment becomes larger and more modal noise is seen in the long (0.5 meters) MMWG than the short (0.25 meters), as expected. However, there is no visible modal dispersion observed due to misalignment. Note that there is the above-mentioned coherent fluctuation, though it decreases in average as dMIS increases. However, there is linear power loss of the signal depending on the misalignment which can be compensated by a simple linear gain stage either in optical or electrical domain. This is an encouraging result, which supports the effectiveness of LTI of MA (thin direct drive type of interface) approach in MMWG system.

In order to understand how an MMWG system performs when it is adopted as part of electrical system through the pair of MAs (i.e., V_{IN} -> MA_{TX} -> MMWG -> MA_{RX} -> V_{OUT}), MATLAB code has been written to simulate and validate signal behavior at each point in the link using the optical transfer function extracted from the EME solver with varied misalignment, $d_{MIS.}$

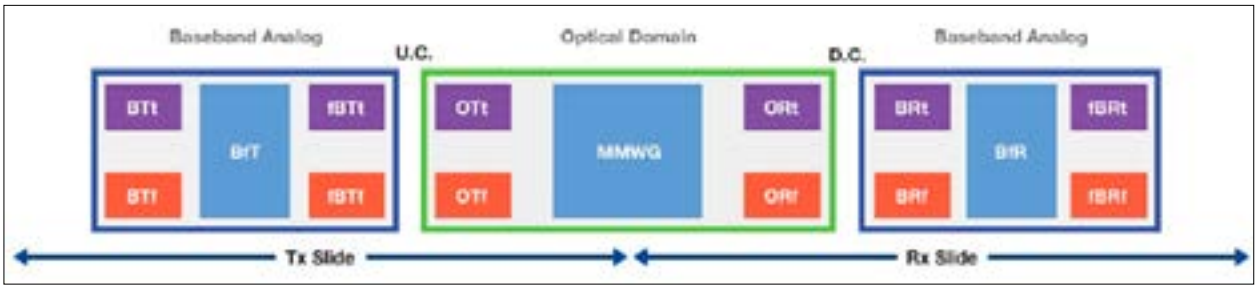


FIGURE 15 - Link Simulation Block Diagram For MMWG System

Figure 15 shows a block diagram for simulation flow in the MATLAB programing, which describes:

(1) Random binary sequence, BTt, is generated as Baseband Tx time signal vector, which can be converted into Frequency domain vector, BTf, through FFT,

(2) BTf vector goes into transfer function of BfT (electrical Baseband Tx filter) and

(3) Converted into optical frequency vector, OTf, at optical domain block through frequency up-conversion (U.C.), which optionally could be expressed for time domain vector, OTt, through iFFT,

(4) OTf then goes into MMWG transfer function to return optical Rx frequency vector, ORf, which optionally could be expressed in time domain signal, ORt, through iFFT,

(5) ORf is down converted at electrical block (baseband analog at Rx side) to BRf as a MMWG output vector in baseband electrical frequency domain,

(6) now, BRf, which optionally could be expressed as time domain signal by iFFT goes through electrical base-band Rx filter, BfR, and finally returns the electrical signal vector in frequency domain in baseband, fBRf, which optionally could be expressed as time domain signal, fBRt.

Figure 16 shows typical link simulation results with snapshots at each simulation point in the link when d_{MIS} =0. Note that 'MMWG zoom out' captures transfer curve over the range of -500THz to +500THz whereas 'MMWG zoom in' does for 352.2THz to 353.2THz which shows details of MMWG S21 as a transfer function (absolute value only).

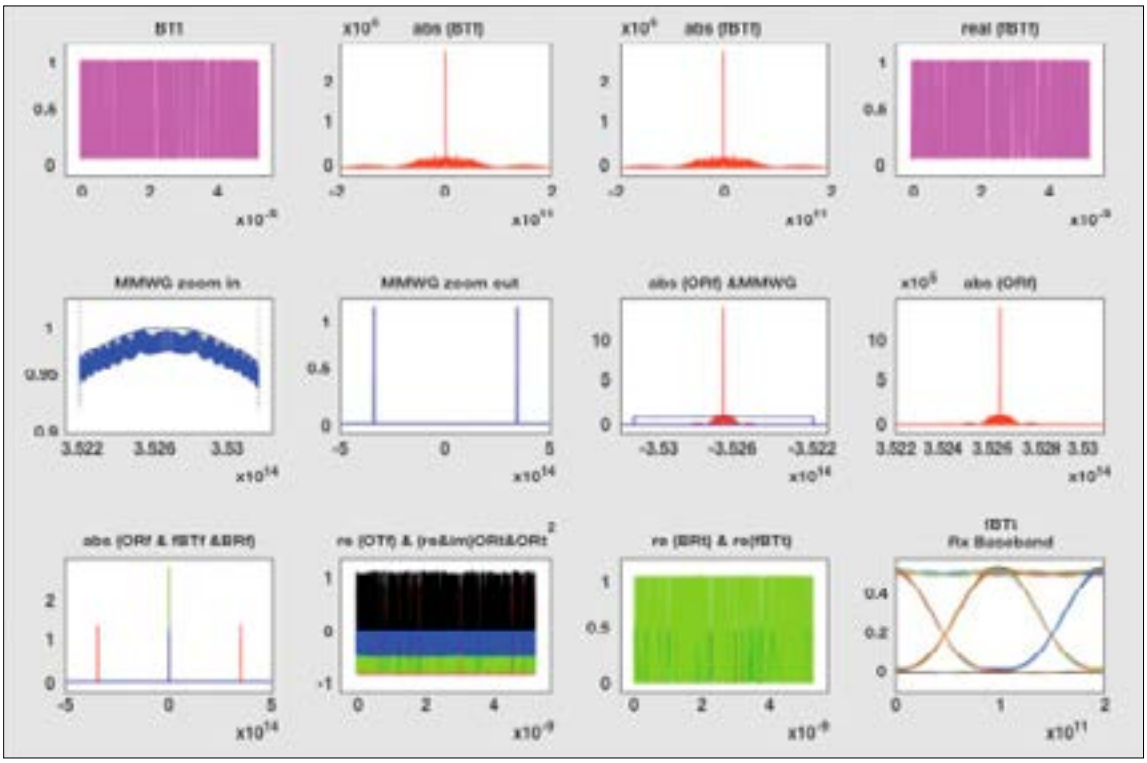


FIGURE 16 - Typical Simulation Results at the Stage Described in Link Model

Multiple MATLAB simulations with various S21 extracted for 0.5 meters MMWG coupled with connector for different d_{MIS} values and with different speed options as well as the addition of linear filters for Tx and Rx are performed and the results are shown in Figure 17. The left most column, Figure 17(a) shows NRZ 100Gbps eye diagrams : The top (Figure 17(a)-1) is with no filter, the middle (Figure 17(a)-2) with Tx gaussian filter of sigma, 2*baud rate (Hz), and the bottom (Figure 17(a)-3) is with same Tx filter and with Rx filter of 0.75*baud rate (Hz) sigma. It is observed that the addition of filters helps to suppress the modal noise through low pass filtering.

The middle column, Figure 17(b) shows results with the same filters set-up as Figure 17(a)-3 case, but with different BR applied. As the speed increases higher cut-off filters are used, but higher order modal noise started to appear increasingly shown in Figure 17(b)-1 for 150Gbps, Figure 17(b)-2 for 200Gbps, and Figure 17(b)-3 for 250Gbps.

The right-most column, Figure 17(c) shows the eye-diagrams when dMIS= 0, 7, 15um for 250Gbps eye diagrams (Figure 17(b)-3). Even with the misalignment increases, the eye-diagram shapes are not changed but eye-height decreases due to the less optical power at the Rx. This is expected from the FIR results (Figure 14).

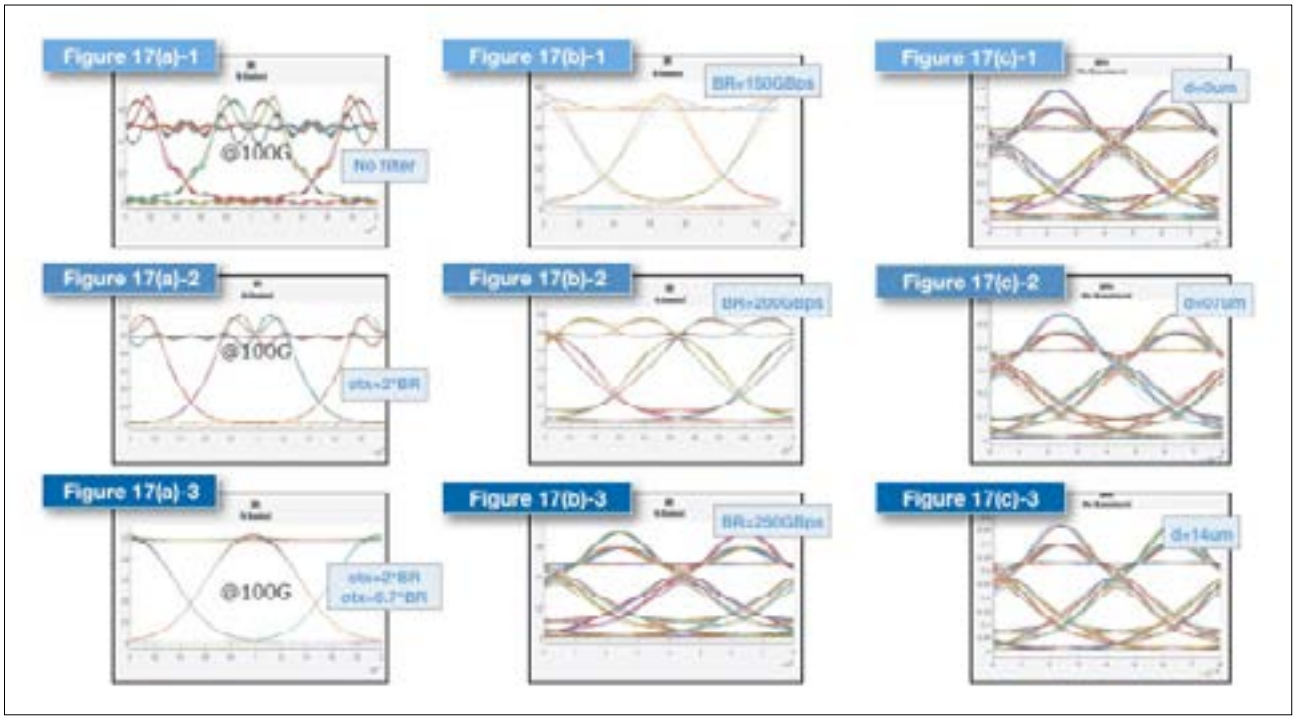


FIGURE 17 - Eye Diagrams for Different dMIS and Speed Options

In summary, the misalignment of optical components does not further affect the modal noise even at higher BR with filters but affects results in the decrease of optical signal amplitude. As mentioned in FIR discussion, this is important because the received impaired waveform can be compensated simply by a linear filter in electrical domain if modal noise is within the specification. In this simulation, we did not include any random noise contributors such as RIN because the link is deterministic noise limited.

Nonetheless, when the speed goes up much higher, the method to suppress the modal noise should be implemented to make the eye opening discernible through possibly the advanced filter technologies such as CTLE, FFE, and DFE in electrical domain, then the random noise should be controlled through device engineering.

Thus, RIN should be considered carefully when it reaches to TDEC (Transmitter and Dispersion Eye Closure) limit, which is yet to be determined after considering all possible remedies, including optical optimization of connector and MMWG and filters, which could be embedded as part of the MMWG link.

5. Conclusion

The increase of electric power consumption in Data Center has been an imminent major challenge. As an engineering solution, we propose a novel interconnection solution called MMWG system, which uses embedded optical waveguides to replace the power-hungry dispersive copper traces. From industry partners we collected some data points for SERDES technologies per subclasses discussed in the major standard bodies. The data shows average slope of EPB (Energy per Bit) per dB of applied SERDES IL (insertion loss), ES_{CU} (EPB slope for Copper Trace IL) = 0.35pJ/bit/dB for 100Gbps SERDES.

With this ES_{CU}, MMWG system can save 114 Watts of power from the switch system of 100G port with the radix of 128 by the removal of 16dB copper IL (for C2M or VSR) and 68W from CPO of 10dB copper IL (from XSR to MMWG) even with 5W additional power due to the directly driven optical interface called MAs (MMWG Adaptors) composed of VCSEL and PD and TIA. As a rule of thumb, if there is copper length of 1.0 dB and higher, then applying MMWG system gives positive power saving balanced out of the addition of MA.

Eye diagram results for both 250mm and 500mm long MMWG cases show no modal noise dependency of the misalignment between the connector and MMWG. This is an encouraging result that the assumed LTI transfer of MMWG system is confirmed being a future-proof solution in bandwidth, power efficiency and footprint challenges beyond CPO.

For higher speed up to 250Gbps, the eye-diagram shows an increase of modal noise. However, since the noise is quite deterministic, advanced filter technologies such as DFE, FFE and CTLE in electrical domain can be further applied for future topics to be reviewed. At the same time, the efforts could also be made on purely passive and optical domain to suppress such noises for the sake of power efficiency.

Also, since the proposed architecture is coupled with conventional copper technology, it is recommended to develop electrical equivalent parameters for MMWG components for the overall ‘figure of merit’ evaluation in conjunction with surrounding SERDES parameters preferably through a standard method, such as Channel Operational Margin (COM) of IEEE 802.3.

6. Terms and Definitions

1. BR - Bit Rate
2. D.C. - Down-conversion
3. EME - Eigen Mode Expansion
4. EPB - Energy Per Bit
5. ES - EPB Slope for IL (pJ/bit/dB)
6. FFT - Fast Fourier Transform
7. FOM - Figure of Merit
8. iFFT - Inverse FFT
9. IL - Insertion Loss
11. LD - Laser Diode
12. LTI - Linear Time Invariant
13. MA - MMWG Adaptor
14. MM - Multimode
15. MMWG - Multimode Waveguide
16. PD - Photo Diode
17. PE - Power Efficiency
18. RI - Refractive Index
19. TCA - Transconductance Amplifier
20. TIA - Transimpedance Amplifier
21. U.C. - Up-conversion
22. VCSEL - Vertical Cavity Surface Emitting Laser

7. References

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