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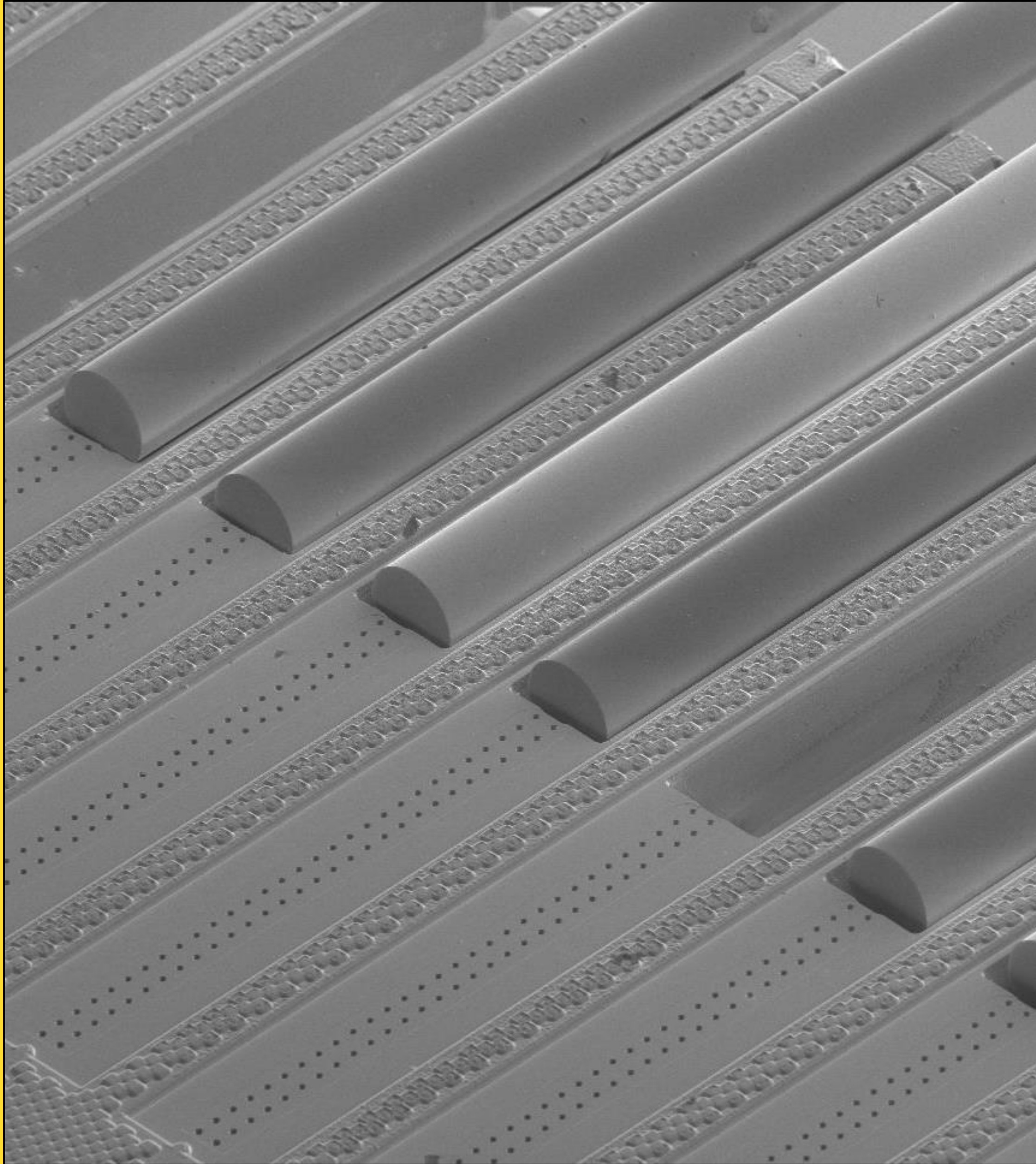
Silicon Photonics: A Foundry & Ecosystem view

Vikas Gupta
Senior Director, Product Management

January 12th, 2024



GF Fotonix™

The "Ecosystem"

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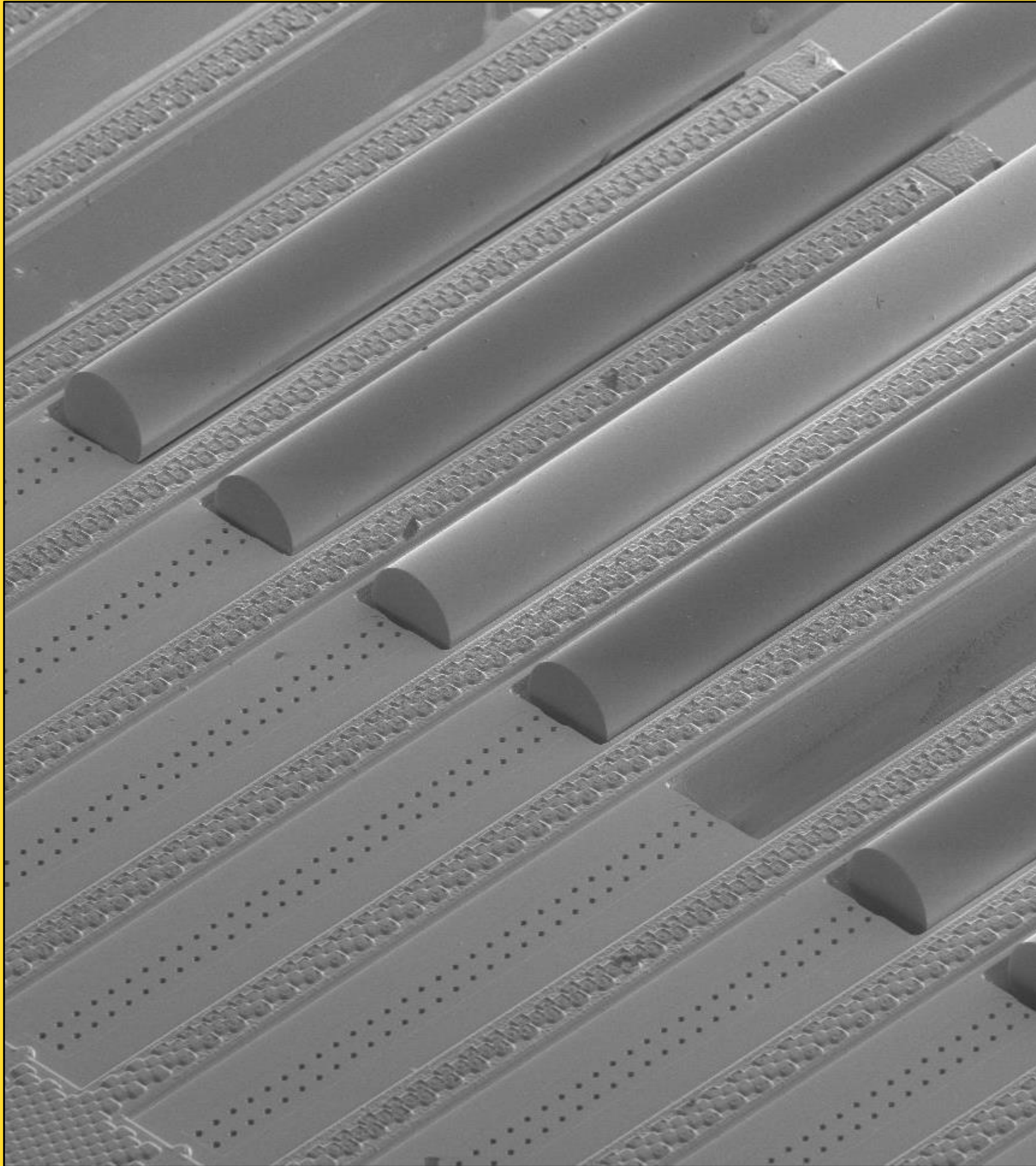

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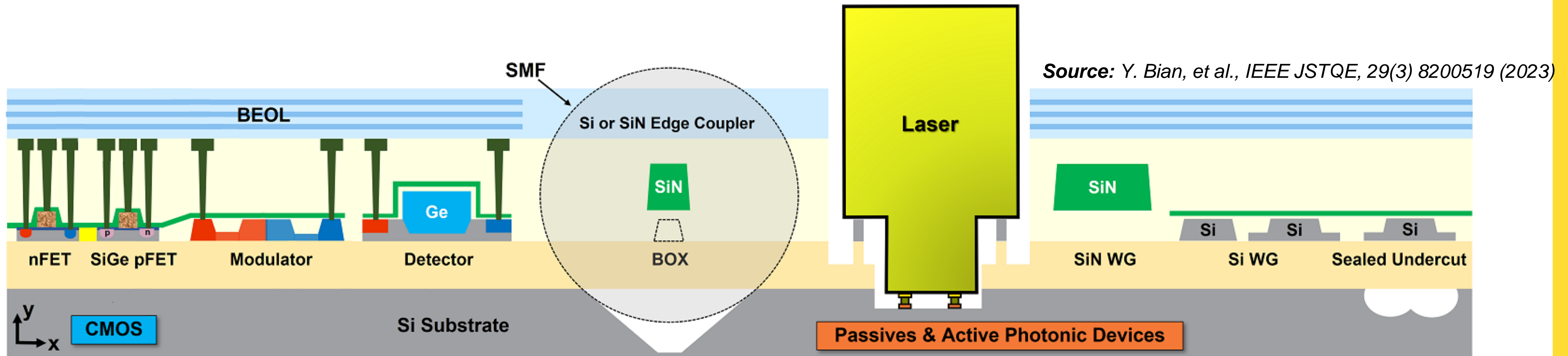
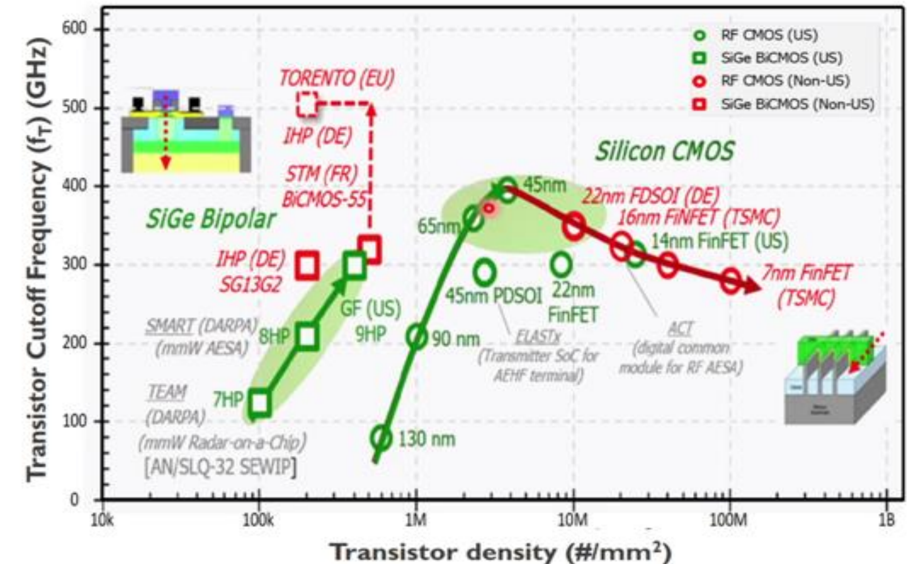
GF Fotonix™: Monolithic Silicon Photonics

Source: Y. Bian, et al., IEEE JSTQE, 29(3) 8200519 (2023)



- **Monolithic** integration of Photonic Devices with a 45nm class RFCMOS
- **300mm** process leveraging immersion lithography
- **Advanced immersion lithography** SOI WGs and photonic OPC
- **Features**:
  - Comprehensive photonic passive device library
  - High performance photonic active devices
  - High efficiency sealed undercut (airgap) thermal heaters
  - Micro-ring modulators and dWDM ring filters
  - Freeform design enabled: accepts custom curve-linear GDS
- **Packaging**: V-groove fiber attach, laser cavity, Cu pillar & TSV
- **Test**: Wafer level state-of-art optical / electrical test capability

https://www.darpa.mil/attachments/T-MUSIC_Proposers%20Day_Jan30.pdf



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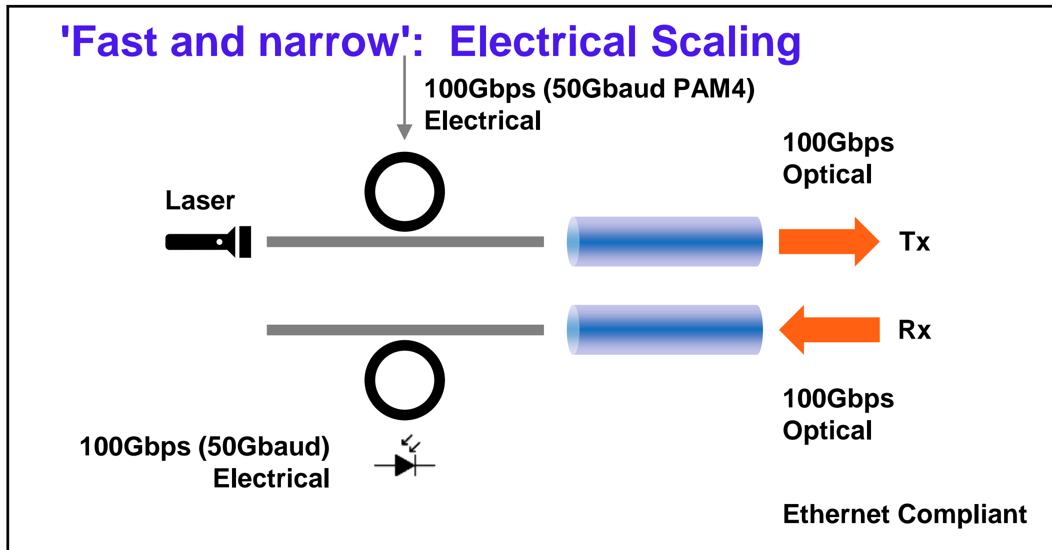
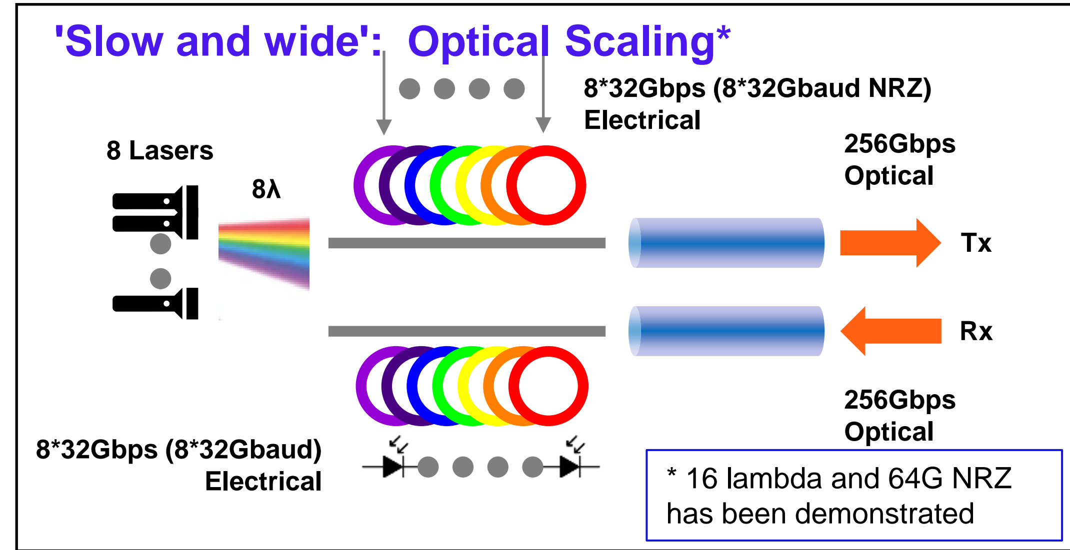
GF Fotonix™: SiPh Architectures





Comments

- Two co-packaged optics architectures showing electrical scale out and optical scale out.
- Both architectures have been developed using the GF Fotonix™ technology (photonics + RFCMOS on single silicon die) and PDK.
- *Either MZM or MRM can be used for 100Gbs and 200Gbs
- Our customers have demonstrated 5pJ/bit power efficiency.

- **AI/ML will continue to drive proprietary modulation scheme and scale out architectures**

- MZM (Mach Zehnder Modulator)
  - Continuous Wave Optical signal is split across two arms of the modulator.
  - Relative optical phase shift across the two arms as a result of electrical signal applied
  - Constructive or destructive interference when the two optical paths are combined results in the imprinting of the electrical signal onto optical.
- MRM (Micro Ring Modulator)
  - Continuous Wave Optical signal on waveguide is coupled into ring
  - Ring is designed to be even wavelengths in diameter
  - Electrical signal is applied to the ring
  - Constructive or destructive interference between the signal on ring vs. on the waveguide results in the imprinting of the electrical signal onto optical

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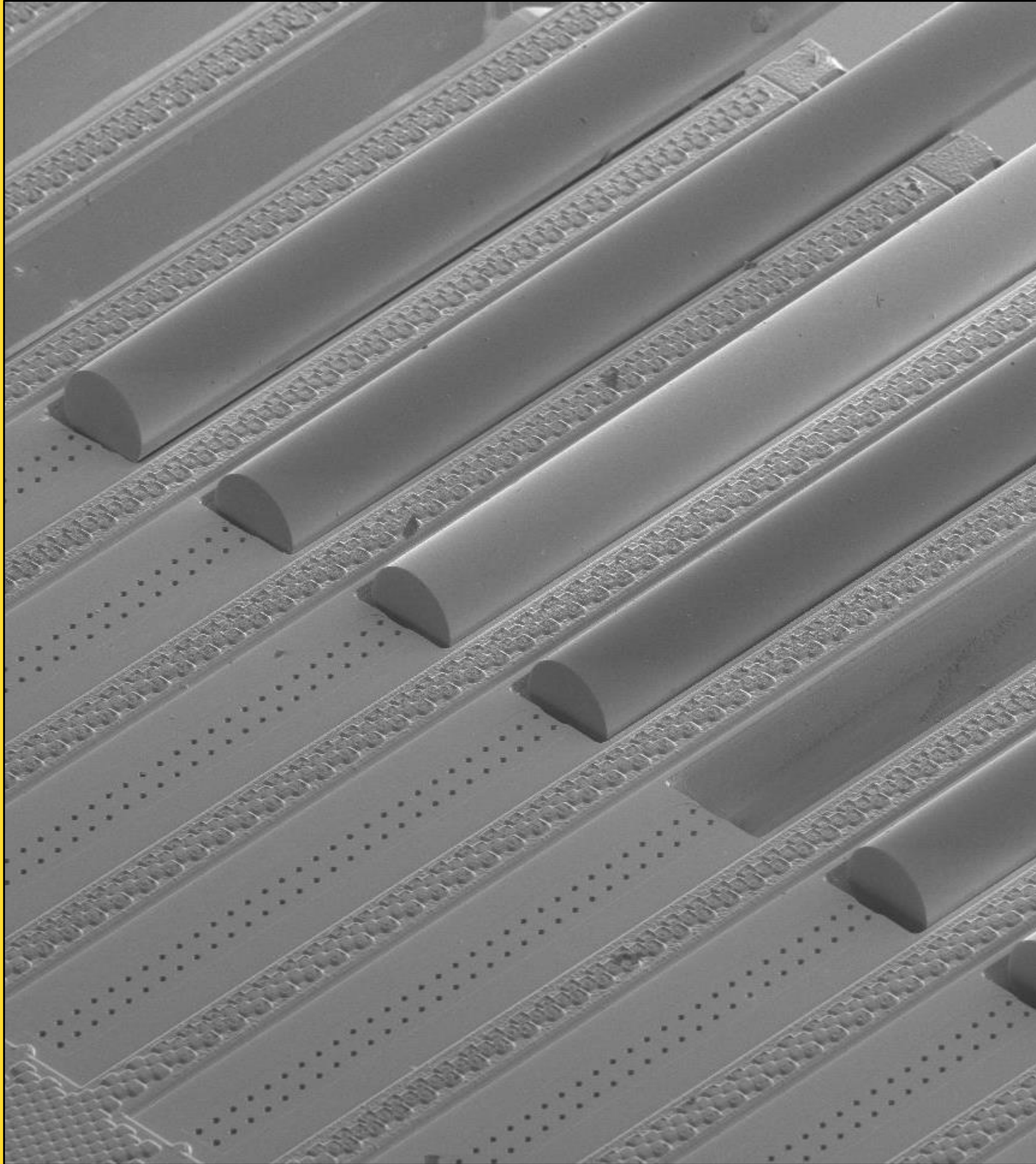

GF Fotonix™

The “Ecosystem”

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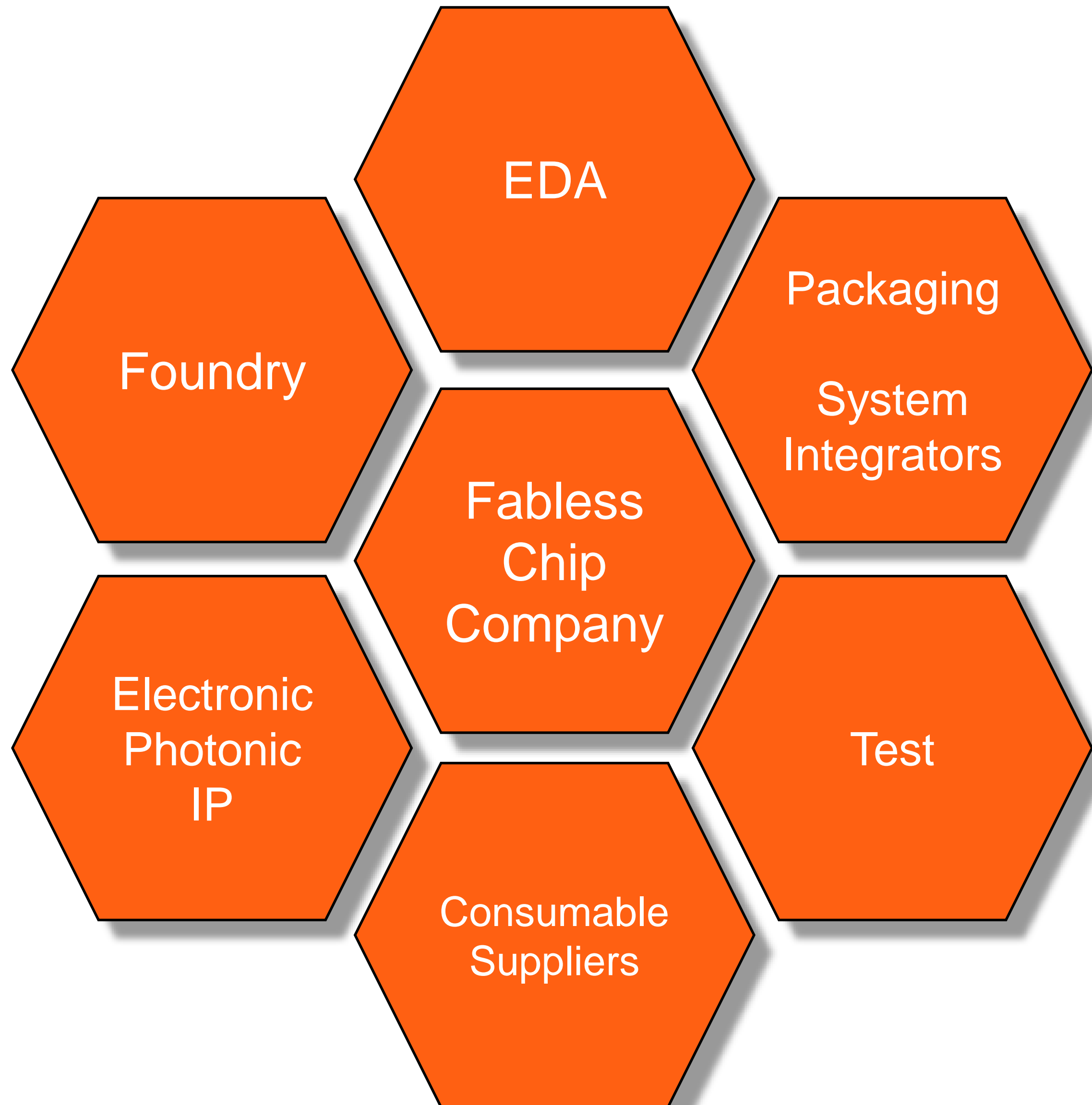
Silicon Photonics "Ecosystem"



ec·o·sys·tem
/ˈēkōˌsistəm/

any **complicated** system consisting of **many different people, processes, activities,** etc., especially relating to technology, and the way that **they affect each other**

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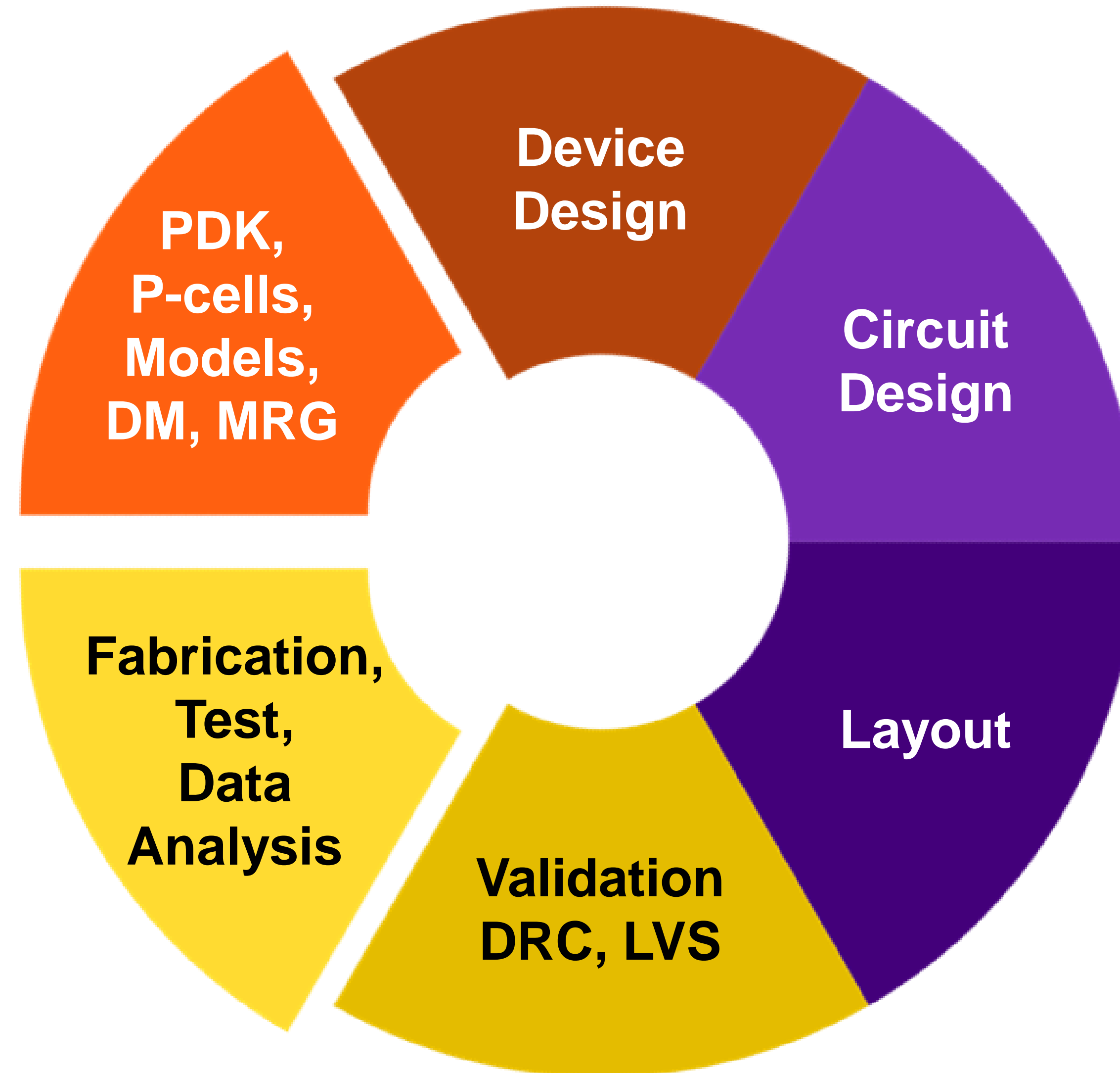
GF Fotonix™: EDA Ecosystem



Ansys

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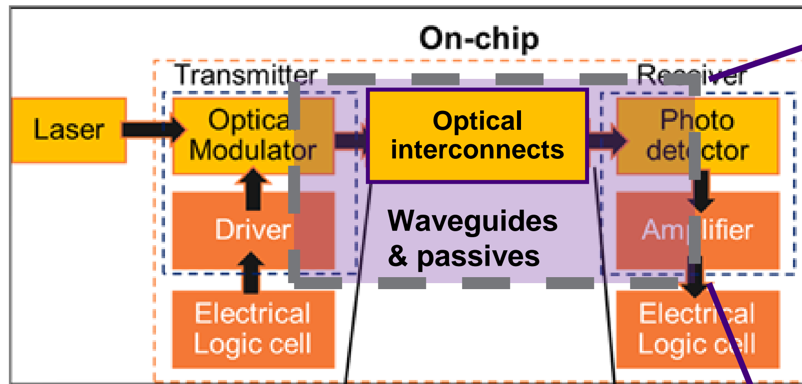
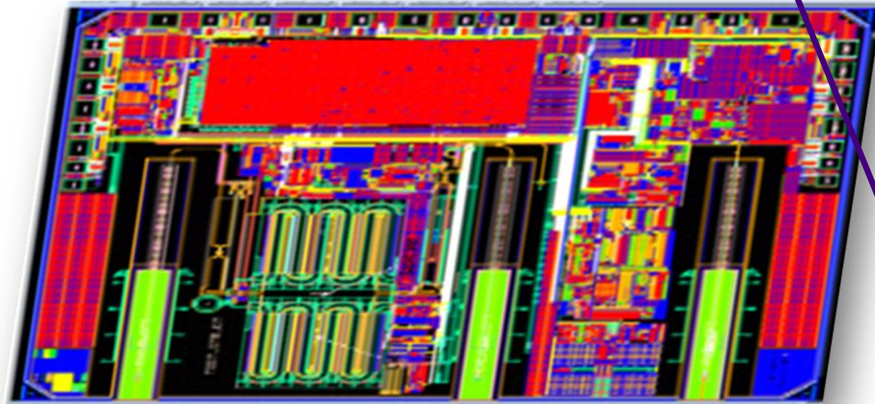
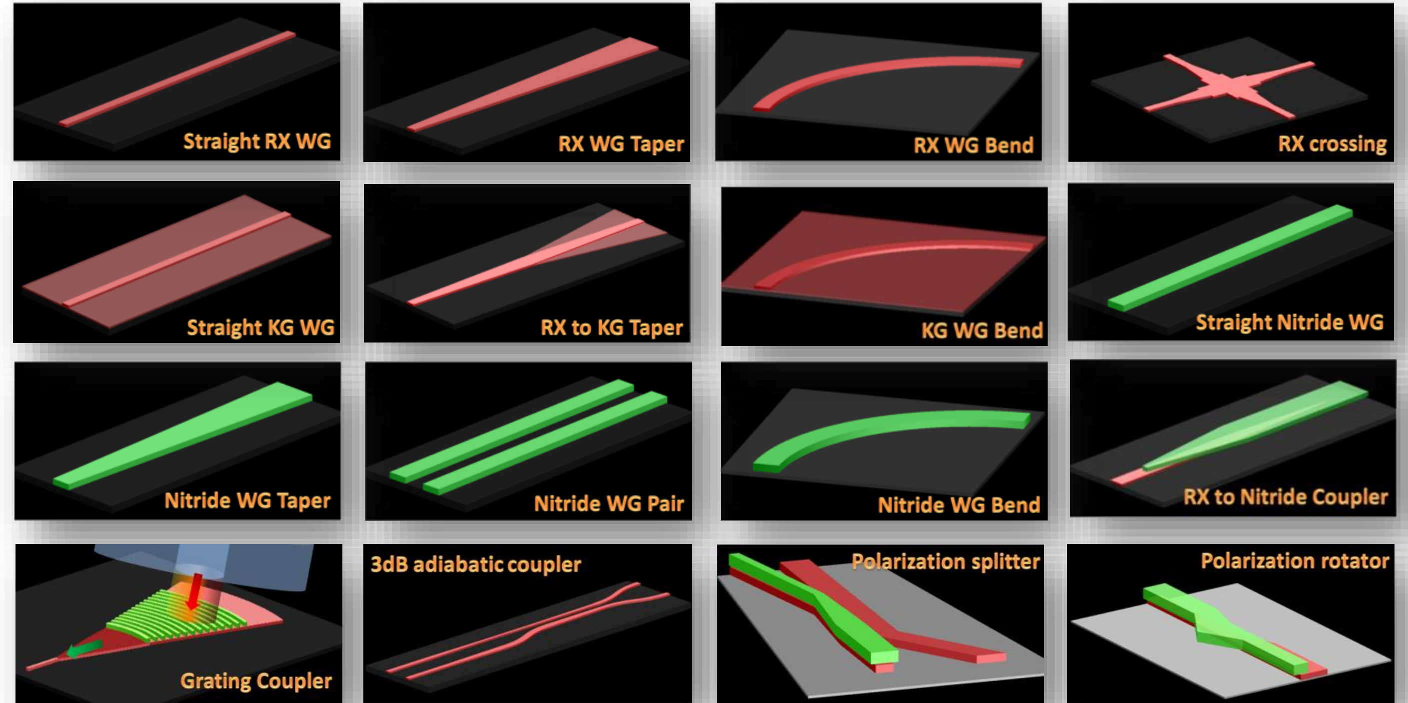
GF Fotonix™ passive library







- Routing, coupling, polarization handling, wavelength filtering, etc.
- Si and SiN-based components

Reference
K. Giewont, et al., IEEE JSTQE, 25(5) 1-11 (2019).
M. Rakowski, et al., OFC, T3H.3 (2020).
Y. Bian, et al., OSA FiO, FW5D.2 (2020).

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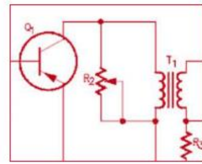
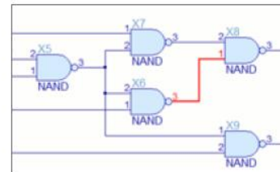
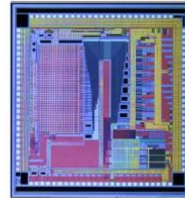
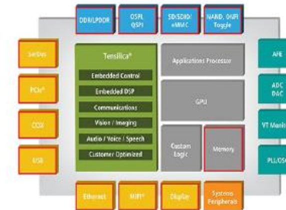
EDA & Packaging

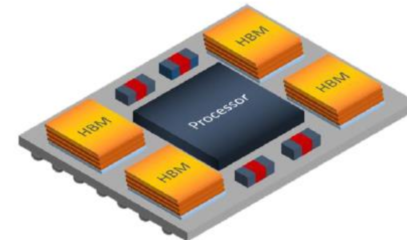
Design is Only Getting Harder…











Transistor-level	Gate-level	ASIC	SoC	Heterogenous Integration
1980	1990	2000	2010	Now
Functional	Functional	Functional	Functional	System-Level
	Timing	Timing	Timing	Functional
		Power	Power	Timing
			Reliability	Power
				Reliability
				Thermal
				Mechanical

This is not your fathers advanced semiconductor packaging…An EDA perspective

John Park (jpark@cadence.com)
Product Management Director – IC Packaging & Cross-Platform Solutions

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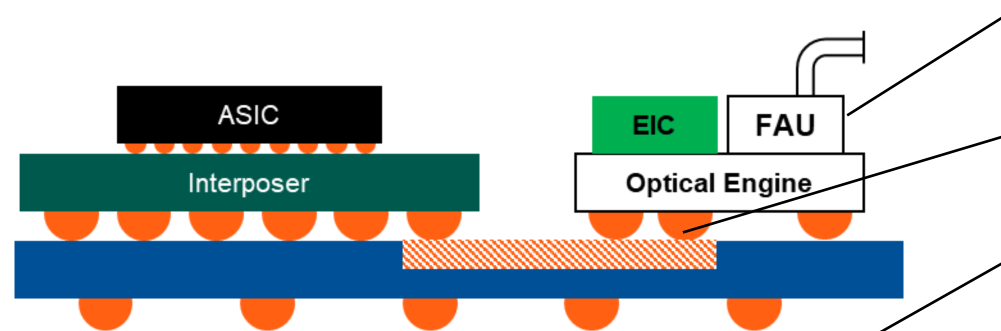
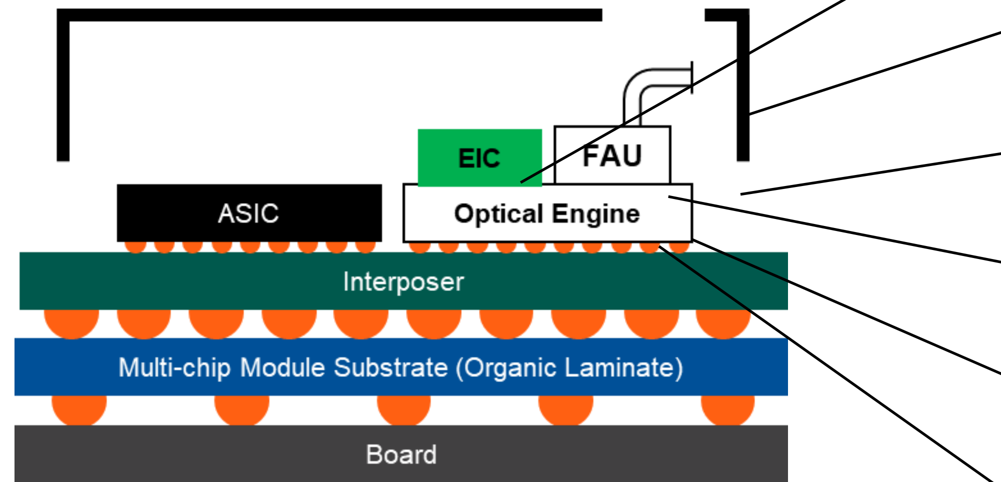
Silicon Photonics Packaging considerations

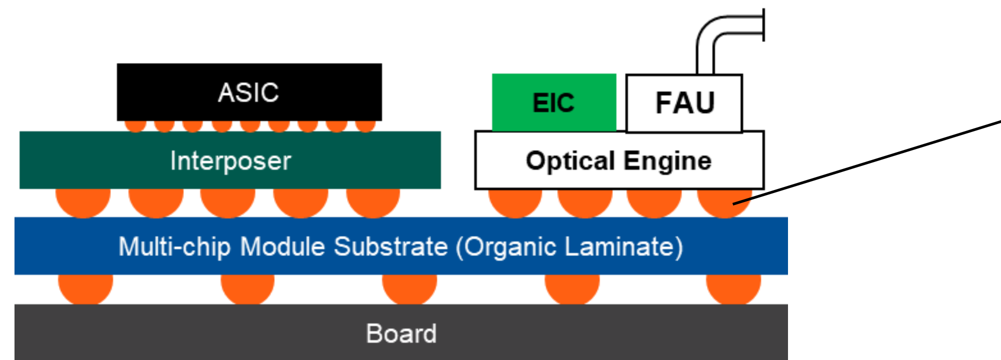
Silicon Bridge



Silicon Interposer



Multi-chip Module (organic laminate)



- FbA (FAU = Fiber attach Unit)
- Mixed pitch Bumps
- Cu Pads or Cu2Cu
- Lidded/Unlidded
- Over Molding
- TSV
- RDL
- μ Bumps
- Bumping

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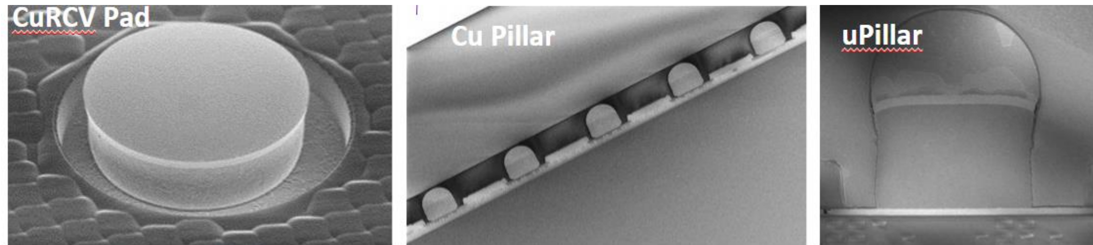
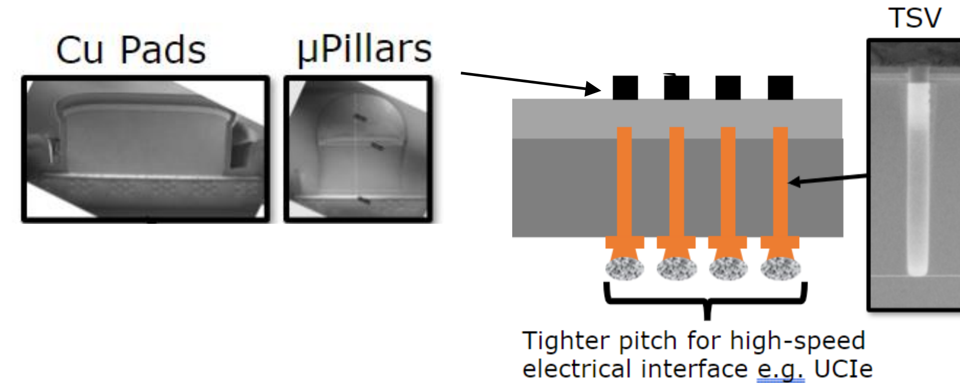
GF Fotonix™: Advanced Packaging

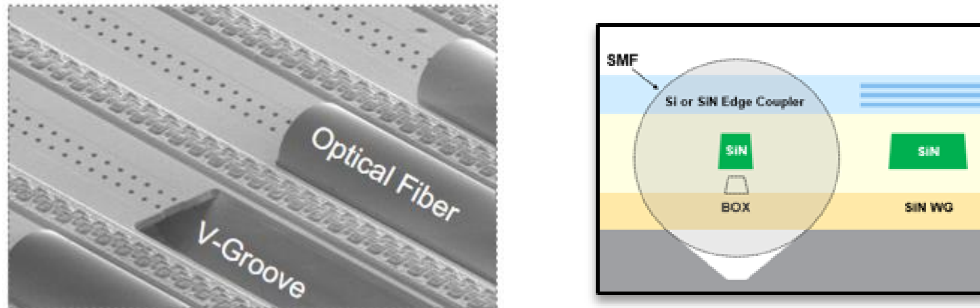
Cu pillar and Cu pillar receive



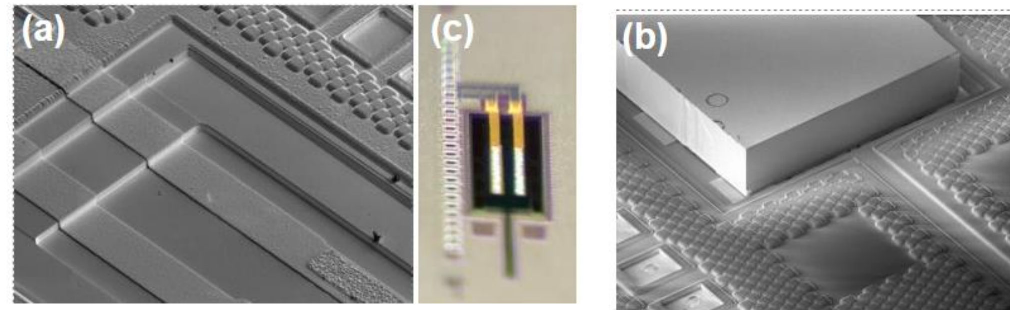
TSV with Cu Pillar



Passive Vgroove fiber attach



Laser cavity direct Laser attach



Silicon Photonics packaging requires integration of novel photonic elements

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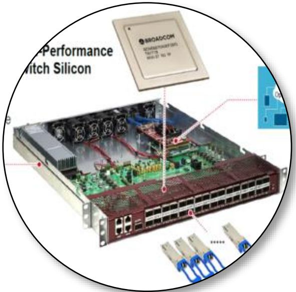
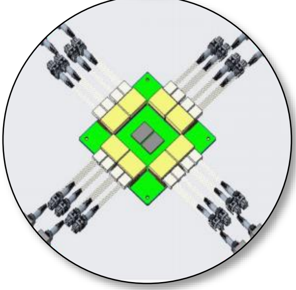
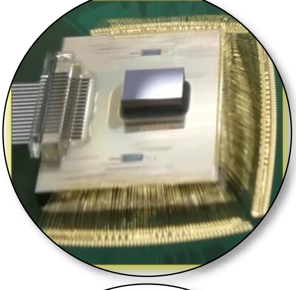
A Challenge: PIC to System Architecture



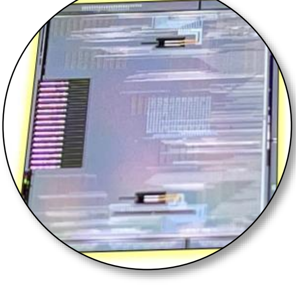
System Build



Module Build



PIC Packaging



Photonic Integrated Circuit

Power Consumption

Electrical – Signal Integrity, Error Correction…

Thermal – Heat Sink, Liquid Cooling…

Space – Fiber turning radius…

Reach

Cost

●
●
●

Mixed pitch bumping/μBumps

Cu Pads or Cu2Cu

Fiber Attach – fixed or detachable

Thru-silicon vias

Redistribution Layers

Interposer, Organic Laminate, Board

Tops Down Approach

Requires early understanding of system requirements to drive choices of PIC technology and corresponding packaging solutions.

Customers will have distinct solutions due to packaging IP

Bottoms Up Approach

Requires non scalable development investments in packaging solutions both for the foundry and OSATs

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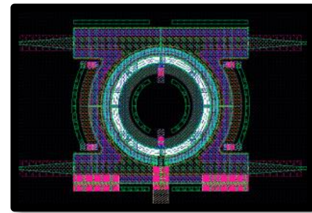
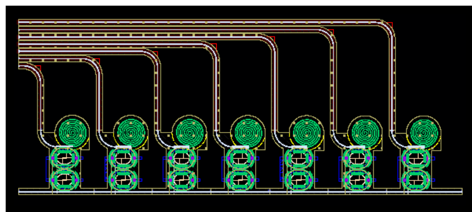
Hierarchical View of Photonic “IP”

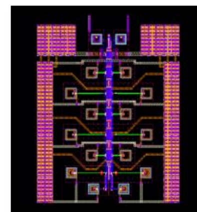


microrings

COMPONENT LEVEL IP

Component IP: Unlike the micro-electronics side, photonic companies continue to innovate on the “device” or “component” side. These devices are expected to be compatible with the foundry process / integration
Delivered through PDK





wdm filters, tia

CIRCUIT LEVEL IP

Circuit level IP: Includes the aggregation of photonic and electronic components. **Examples:**

- Photonic Circuit: dWDM filter
- Electronic Circuit: TIA, Drivers, DAC/ADC
- EO Circuits: dWDM filter with heater controls

Delivered through IP Eco-system or through design services

Chiplets

CHIPLET LEVEL IP

Chiplet IP: Example: 800G CPO meeting DR8 specs on optical side with direct drive or PCIe compliance on electrical side
Delivered from Fabless Design Houses

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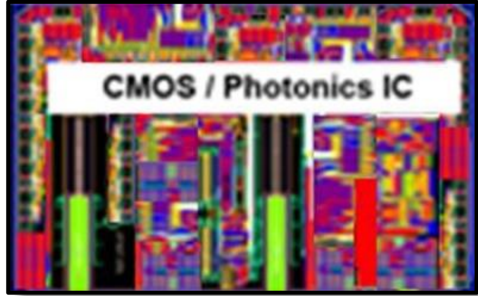
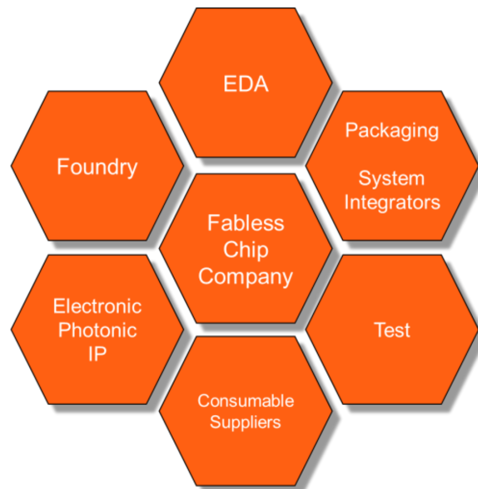
In summary



GF Fotonix™ is a high differentiated, feature rich silicon photonics platform with the flexibility to support CWDM & dWDM solutions



Silicon Photonics requires a vibrant ecosystem to reach its full potential.
The ecosystem includes EDA, IP, OSAT, Test and supplier engagement

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