OPTICA
Formerly OSA

ADVANCED PHOTONICS COALITION

QUANTIFI PHOTONICS™

SCALING INTEGRATED PHOTONICS FOR THE AI REVOLUTION - A TESTING PERSPECTIVE

Integrated Photonics Ecosystem Series

Kees Propstra

OUTLINE

Problem statement

Photonics test overview

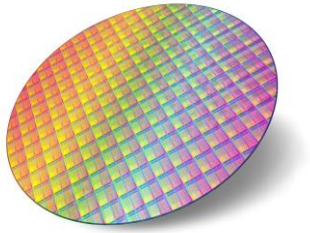
Examples

Conclusions

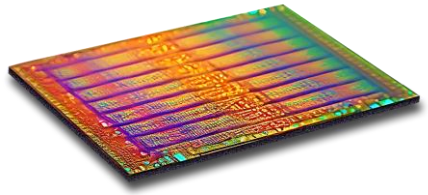
Bechtolsheim, PECC Summit'23

PROBLEM STATEMENT

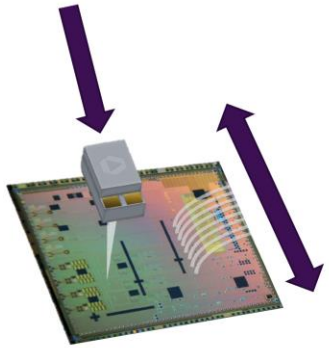
Production Stages



Wafer Sort



Die/PIC



Assembly

Packaged Test

Product Life Cycle

DEVELOPMENT (R&D) → VALIDATION (DVT) → MANUFACTURING → DEPLOYMENT

PHOTONIC DEVICES OVERVIEW

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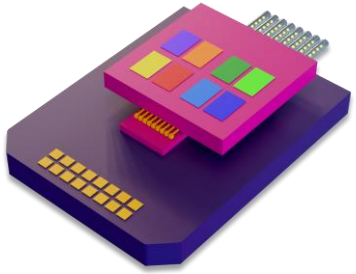
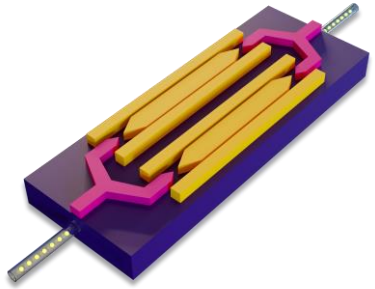
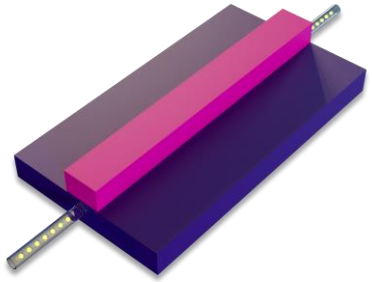


External Laser Source

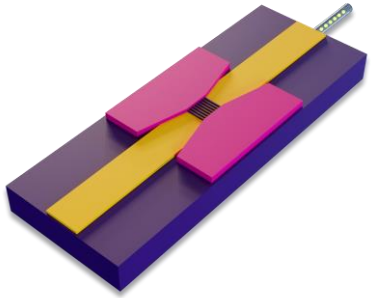


Modulator

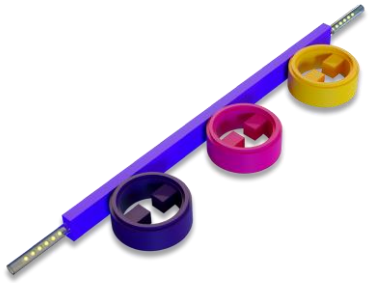


Waveguide

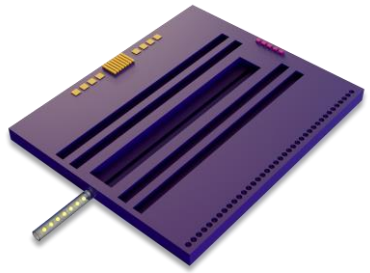
Grating Coupler



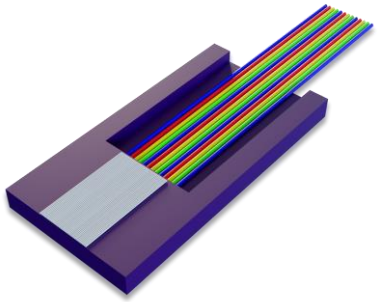
Laser Diode



Ring Resonator



Receiver



Fiber Array

MEASUREMENTS OVERVIEW

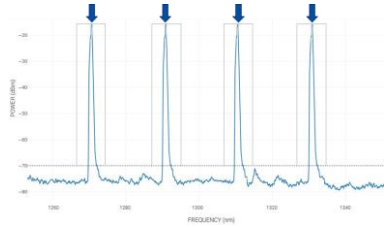
Passive

Insertion loss

Return loss

Wavelength dependence

Polarization dependence



Waveguides
Mux/demux
Grating coupler

Active

Fiber array alignment

Power levels

Optical spectrum/SMSR/OSNR

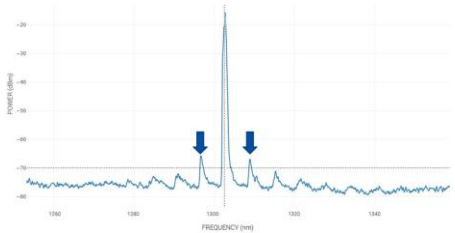
Line width

Modulation depth

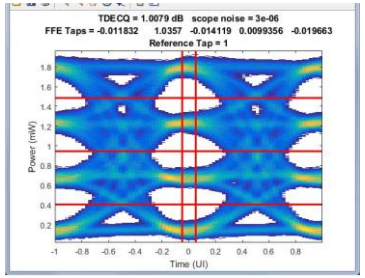
LIV-curve

Photocurrent/linearity/responsivity

RIN measurement



Laser diode
Ring resonator
Modulator
Receiver
Fiber array



High-speed

Eye diagram

BER

Receiver sensitivity

S-parameters

Modulator
Receiver
Module

INSTRUMENTS OVERVIEW

Input

Fixed Laser

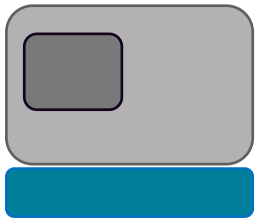
CW-CWDM ELS

Tunable Laser Swept or Step

POL Controller

Broadband Source (LED)

Output



LCA

OPM

DSO

OSA

Photo Current Amplifier & Meter

BERT

O2E

Support

Optical Amplifier

VOA

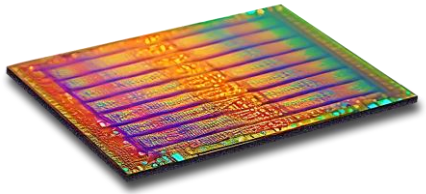
50/50 Splitter

1xN Switch

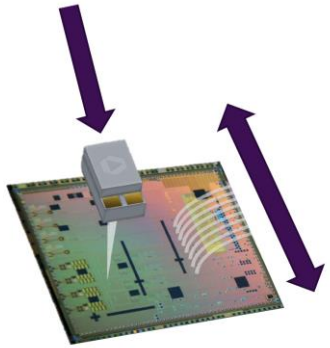
SMU

VST

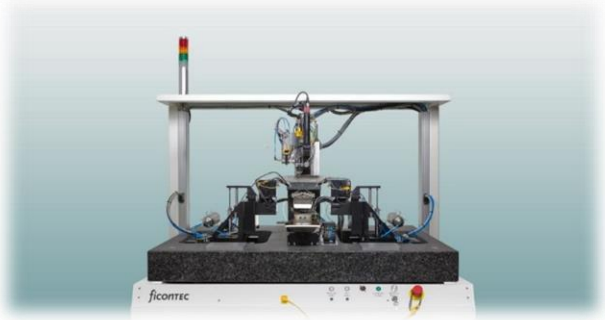
WHAT TO TEST WHEN?



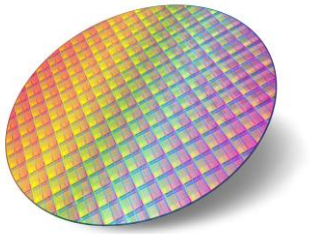
Die/PIC



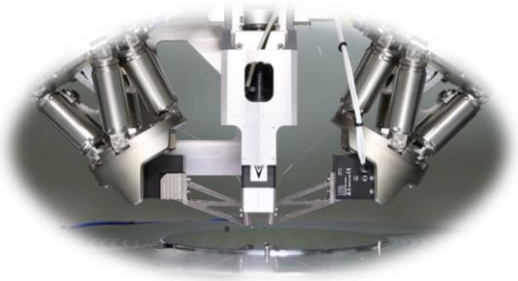
Assembly



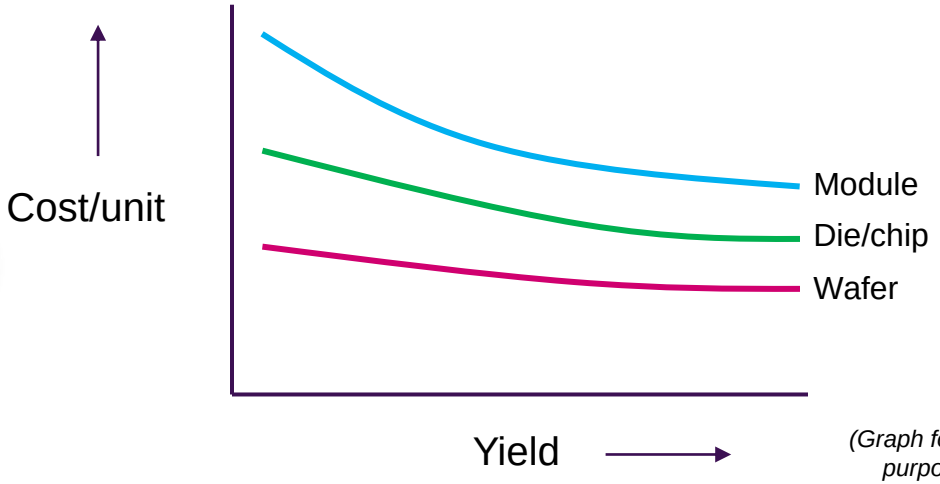
?



Wafer Sort

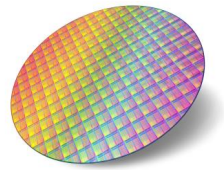


Packaged Test



(Graph for illustration purposes only)

WAFER LEVEL INSPECTION/TESTING



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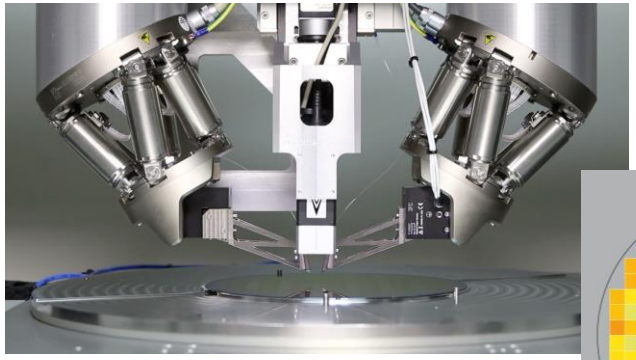
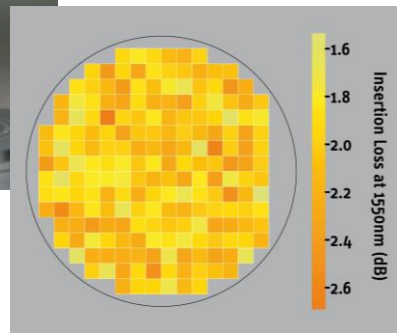
Parametric testing - wavelength and polarization dependent behavior

Setup with wafer handler and a probing system:

- Inject the optical signal into the wafer
- Power and activate DUTs
- Measure the optical signal out of the DUT
- High-speed characterization desired (known-good-die)





FIRST PHASE (pre-production)

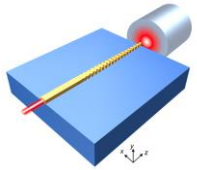
Cover all performance parameters (including high-speed) to guarantee known-good-die.

SECOND PHASE (production)

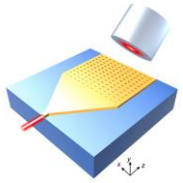
Cover most performance parameters, based on statistical sampling to guarantee known-good-die.

DATA CORRELATION

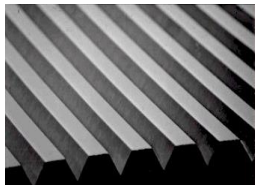
- Reduce the number of different tests (scale down test coverage)
- Reduce the percentage of devices tested
- Front load the testing (product life cycle, manufacturing stages)



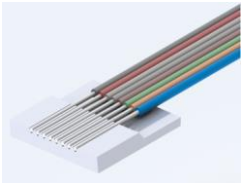
Edge Coupling



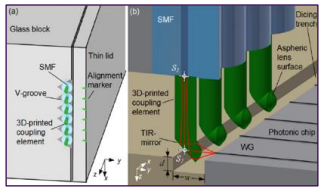
Grating Coupling



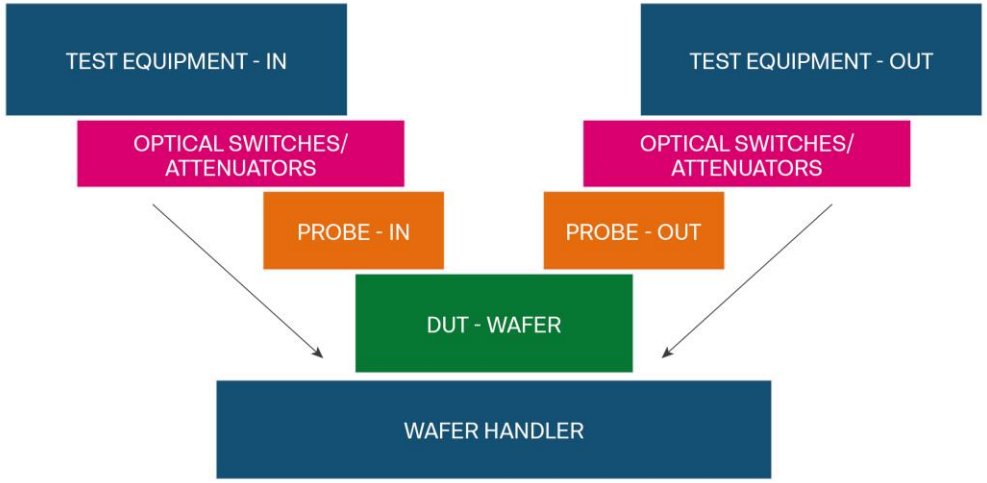
V-grooves



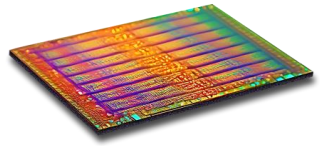
Fiber Array Unit



3D-printed lens periscopes



DIE/PIC- FIBER ARRAY ALIGNMENT AND ASSEMBLY



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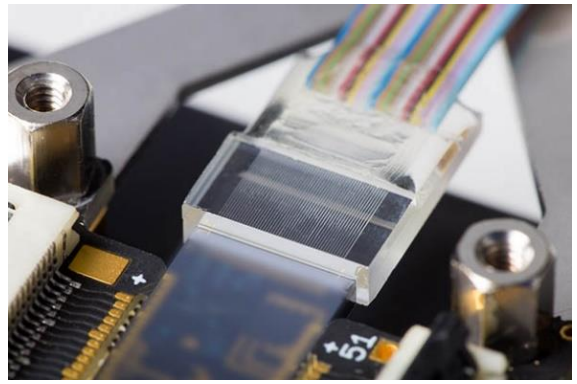
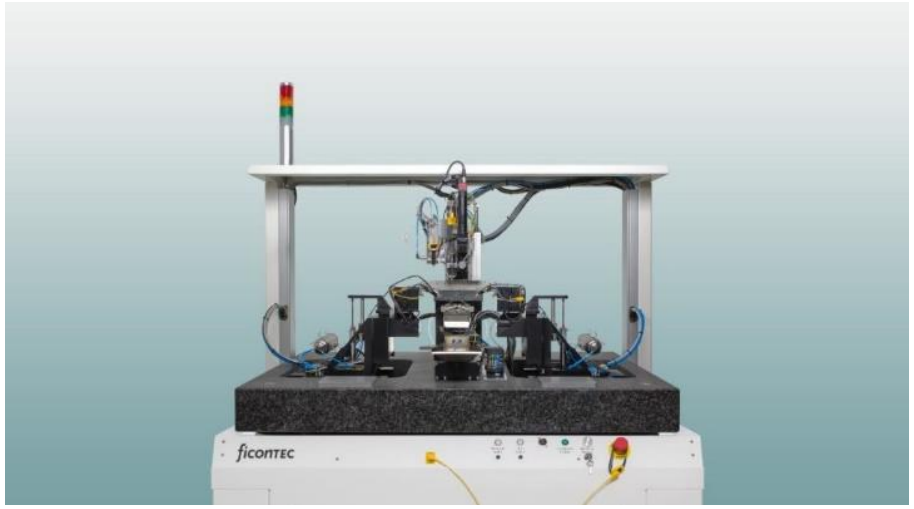
Guaranteed known-good-die from previous stage

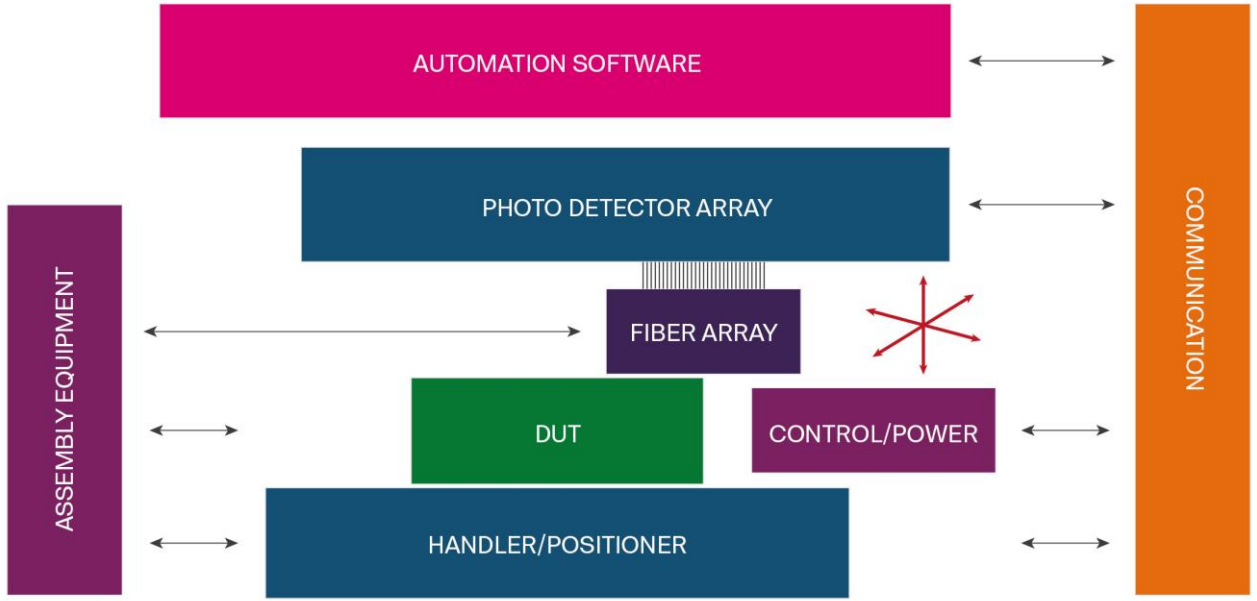
- Perform fiber array alignment and other assembly steps
- Optimum fiber array position while curing the adhesive between DUT and fiber array
- High yield, low risk - validating that all channels of the DUT are still performing within spec
  - Parallel testing for quick screen
- If assembly steps are lower yield (higher risk) then other tests may be appropriate



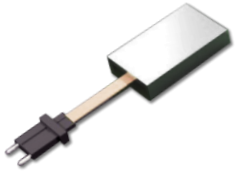
288 channel optical power meter

Power-1410-288-MTP-EPIQ





MODULE TESTING



Final step of the manufacturing cycle

- At-speed optimization and test for spec compliance
- MSA form factor QSFP-DD, OSFP-XD, OIF 3.2T CPO
- Test fixture for DUT control and high-speed signal access
- Thermal stream or TEC for temperature control
- Final tweaking of device parameters to maximize yield

FIRST PHASE (pre-production)

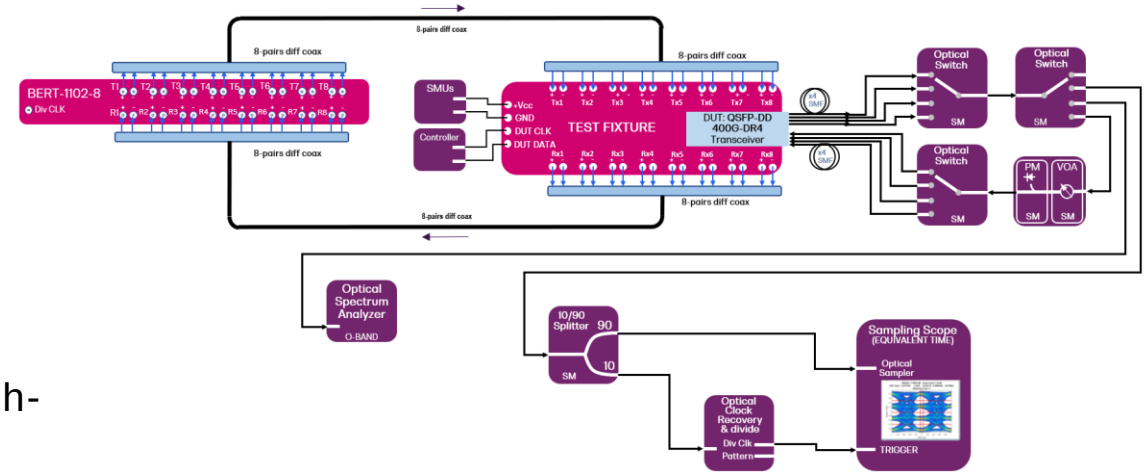
Cover all performance parameters to guarantee product meets all requirements *over temperature.*

SECOND PHASE (production)

Cover most performance parameters to guarantee product meets all requirements. Thermal validation hopefully can be avoided in the high-volume stage.

DATA CORRELATION

- Scale down test coverage
- 100% testing (devices/channels) still seems desirable
    - Parallel testing!



RECIPE FOR SUCCESS

FULL COMPLEMENT of photonics test functions

FLEXIBLE platform to transition from R&D to validation/characterization, pilot and finally mass production

INTEGRATION into wafer probing, assembly and alignment equipment

SCALABLE to high-channel-count parallel testing

HIGH-DENSITY to pack a lot of test instruments in a small space

OPTIMIZED test flow (time is money)

ECOSYSTEM ASKS

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STANDARDIZATION desired/required?

Optical signal access

Measurements and test plan

Hardware framework

Powered by PXI Systems Alliance

Software framework

gRPC

* Images courtesy of ficonTEC