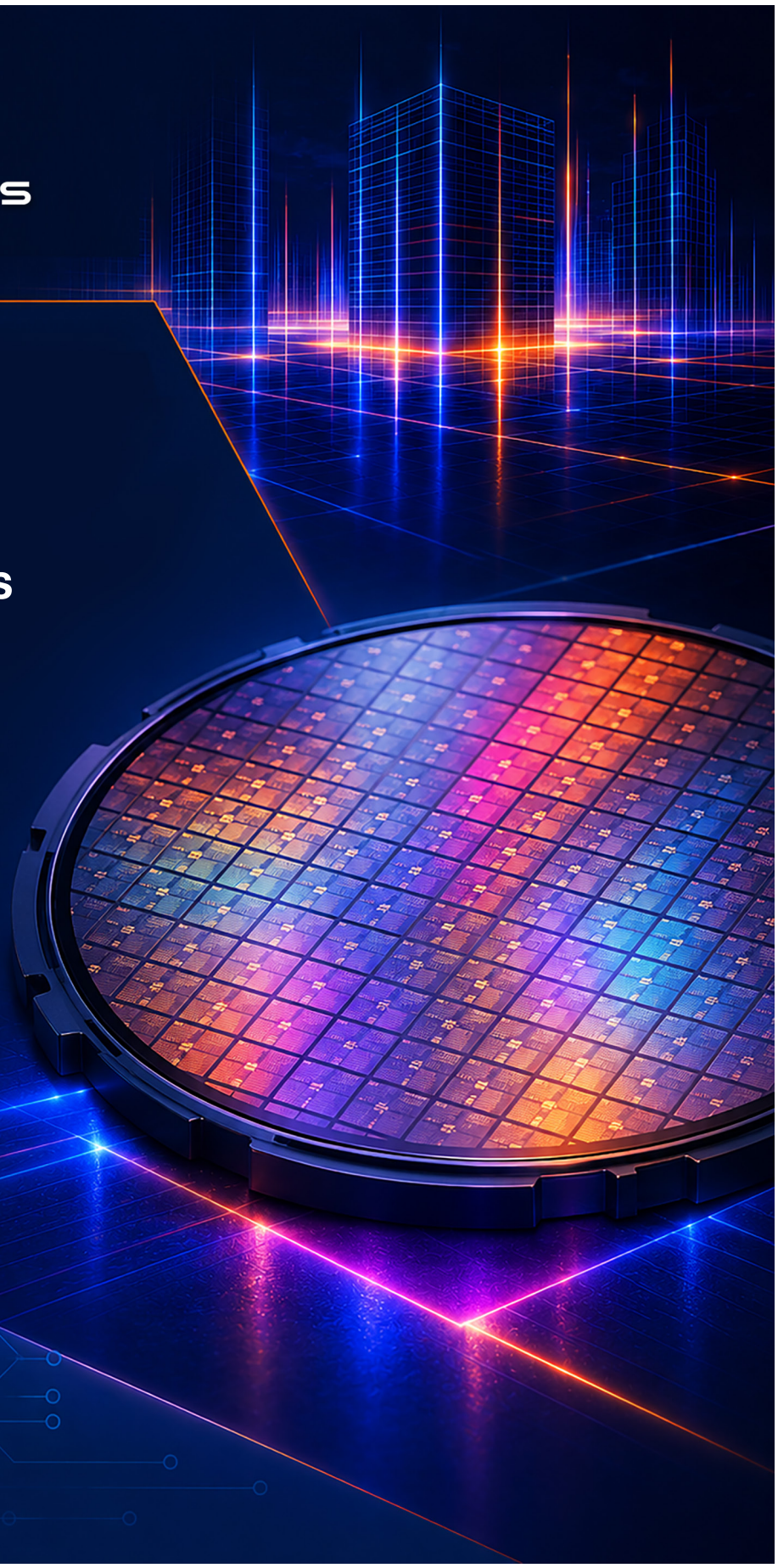
ADVANCED PHOTONICS COALITION

Silicon Photonics Manufacturing Specification

VERSION 1.0



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1. Introduction

Silicon photonics has moved from a specialized telecommunications technology into a foundational manufacturing discipline for next-generation computing infrastructure. The combination of explosive AI workload growth, ever-larger accelerator clusters, and the physical limits of copper electrical interconnects is pushing co-packaged optics (CPO) and silicon photonic integrated circuits (PICs) into the critical path of data center design. This specification provides a detailed technical overview of silicon photonics manufacturing as Advanced Photonics Coalition's Silicon Photonics Manufacturing Standards Working Group addresses scalable, lower-cost, high-volume manufacturing methods as the priority of the working group's mission.

1.1 Silicon Photonics Overview

Silicon photonics, which integrates optical components onto semiconductor chips, is expected to generate at least $46.5 billion in revenue by 2035 and is increasingly seen as a key technology for emerging applications, including artificial intelligence and quantum computing. While demand is expected to grow, particularly in AI and quantum applications, the pace of development depends on improving access to infrastructure and reducing bottlenecks in the supply chain.

Silicon photonics uses CMOS-compatible wafer fabrication processes to build optical waveguides, modulators, and detectors on or near silicon substrates. Silicon Photonics inherits decades of CMOS process maturity, wafer-scale economics, and an existing base of high-volume fabs. This is a positive development for supply security utilizing each foundry's process design kit, integration philosophy, and packaging roadmap. Without active industry coordination, the Silicon Photonics Ecosystem risks fragmenting into incompatible, vendor-specific design flows.

Process design kits (PDKs) are the foundry-provided libraries of validated components, design rules, and simulation models that allow fabless photonic IC designers to target a given foundry process with predictable results. PDK maturity, validated component breadth, and portability across foundries are central determining factors of how quickly new entrants bring silicon photonic products to market. Advanced Photonics Coalition (APC) Open Ecosystem is an initiative where shared best-practice guidance can meaningfully shorten design cycles across the industry.

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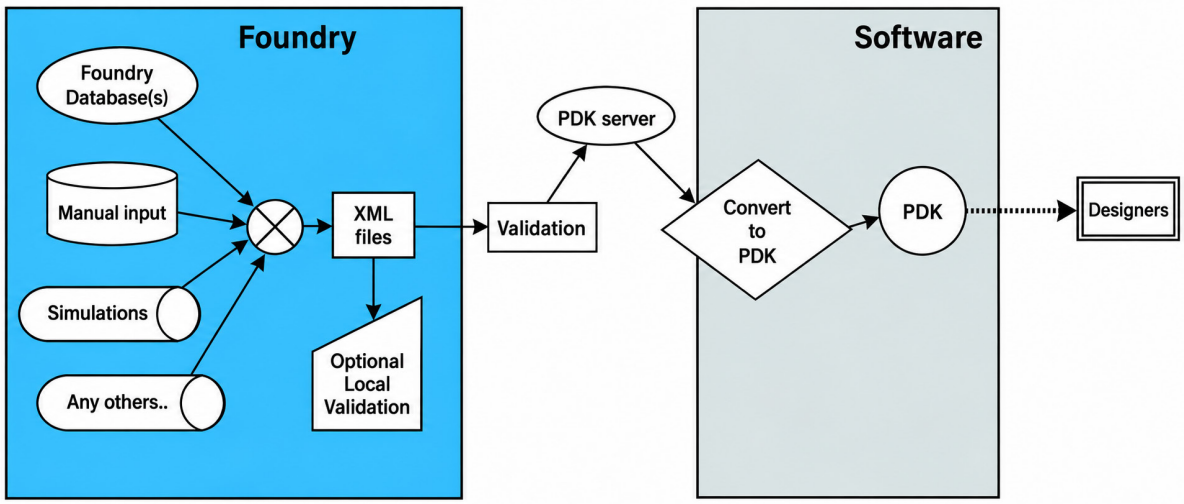

Figure 1 – Process Design Kits (PDKs) are Foundry-Provided Libraries.

Co-packaged optics depends on advanced packaging techniques originally developed for high-performance electronic chiplets. Layered onto these electronic packaging techniques are photonics-specific steps, most notably fiber attach, where optical fibers or fiber arrays must be aligned to on-chip waveguides to sub-micron tolerances and permanently secured, using either active alignment or passive, self-aligned mechanical structures designed into the chip and substrate.

Two integration philosophies dominate current foundry roadmaps: on- lasers and external laser sources optically coupled into the photonic circuit.

For Silicon Photonics testing, wafer-level optical probing requires precision fiber or free-space optical coupling to devices that have not yet been packaged. Burn in and accelerated life testing for hybrid-integrated lasers must account for failure modes that have no electronic equivalent. This specification offers reliability qualification standards developed for telecommunications-grade components and establishes qualification methodology appropriate for prototyping and high-volume data-center-scale deployment.

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1.2 Supply Chain Ecosystem Driven Standards

The below represents the sectors of the Advanced Photonics Coalition Silicon Photonics Supply Chain Ecosystem Driven Standards:

Figure 2 – Advanced Photonics Coalition Supply Chain Open Ecosystem Driven Standards

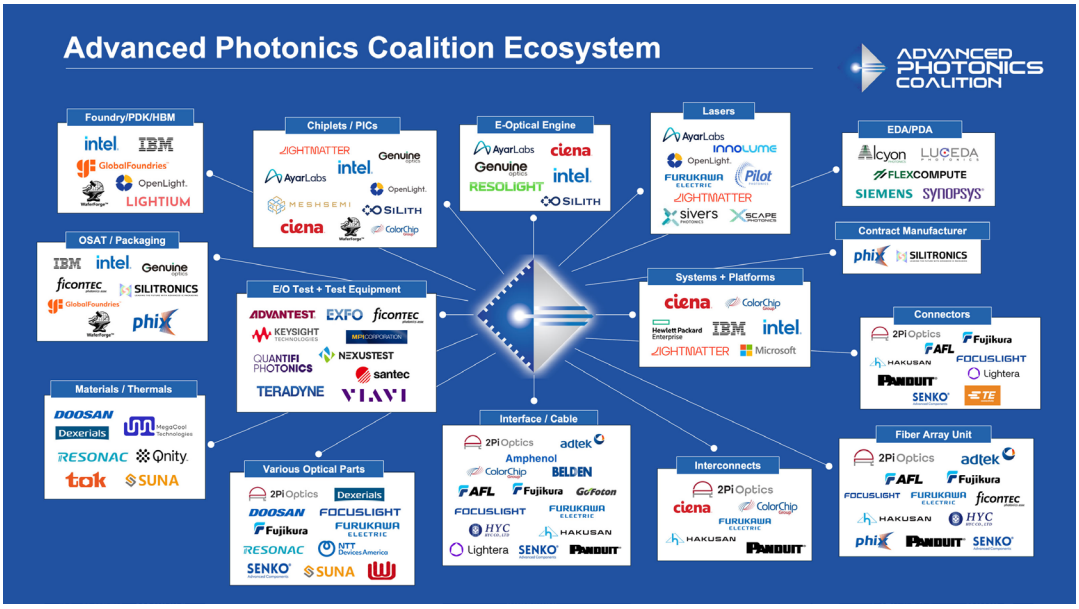

Figure 3 – Advanced Photonics Coalition Standards Member Ecosystem as Oct. 2026

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2.0 Mechanical & Coupling Photonics Interface

Section 2 “Mechanical & Coupling Photonics Interface” addresses the standardization requirements of current photonics device manufacturers across the global value supply chain, spanning Photonic Integrated Circuit (PIC) and Electrical Interface Chip (EIC) design companies, component suppliers, photonics foundries, Outsourced Semiconductor Assembly and Test (OSAT), system integrators, and hyperscale data center operators.

The primary application domains targeted are high performance computing (HPC) and artificial intelligence (AI), where interconnect performance between compute dies and devices has become a critical bottleneck. As traditional copper-based interconnections approach their physical and performance limits, standardized photonic mechanical and coupling interfaces are essential to enable scalable and interoperable system architectures.

A comprehensive catalog of optical coupling approaches is developed from an OSAT perspective, covering both mechanical and optical aspects. Each configuration is analyzed to identify key differentiating parameters relevant to design, assembly and test.

This section defines essential geometrical dimensions directly impacting PIC layout and system integration. Critical design parameters and their associated tolerances are defined to enable standardized, robust, and mutually compatible optical coupling sites. In parallel, optical components and integrated connector types will be categorized, with associated performance and reliability metrics established.

Cleanliness and contamination requirements are addressed as fundamental enablers of optical performance. Industry relevant contamination control parameters are proposed and adapted to photonic integration as standardized specifications.

Reflowability constraints within the optical interconnect context will be clarified and documented.

Finally, this section represents an ongoing, collaborative effort, relying on active input from committee members to define and implement practical industry standards.

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2.1. Light Coupling Definition

In the context of silicon photonics and opto-electronics such as Co-Packaged Optics, Linear Pluggable Optics, Near-Packaged Optics or any optical technology, **light coupling** refers to the integration of optical interfaces and components within the device package to enable controlled and efficient transfer of optical signals between an external optical medium, such as optical fiber, and an on-chip waveguide integrated within a PIC die, and vice versa.

Light coupling encompasses the optical, mechanical, and alignment mechanisms necessary to accommodate disparities in optical mode characteristics for spot size converters using mode field diameter (MFD), numerical aperture (NA), and propagation geometry, between the coupled media. A significant difference typically exists between the mode field diameter of a standard single-mode optical fiber and that of a silicon waveguide embedded in a silicon-oxide cladding, with representative values on the order of 9 µm and 0.7 µm, respectively. This mismatch drives the need for standardized coupling structures and precise mechanical interfaces.

Figure 4 illustrates various optical schemes for fiber to PIC light coupling. Each of these solutions, when implemented, requires some packaging technology to ensure mechanical precision and robustness, as well as the maintaining of a low optical loss under environmental stress. It is the role of the OSAT to develop the technology for this necessity.

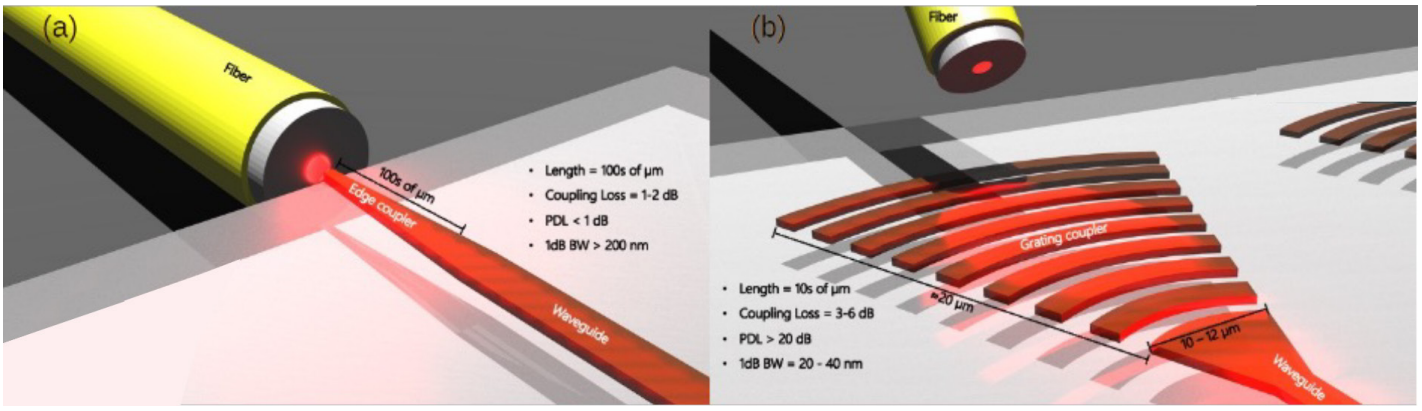

Figure 4 – (a) Schematic view of a single channel edge coupling from a fiber to an integrated waveguide (b) Surface light coupling with a grating coupler. In a real assembly, the fiber angle and distance must be fixed.

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2.2. Packaging Categories

Depending on the technical requirements of the photonic devices, several light-coupling strategies are implemented at the package level. The objective of these Advanced Photonics Coalition standards is to clearly define and categorize these approaches according to well-established coupling configurations. A summary of these categories is presented in Figure 5 and will be further explained below.

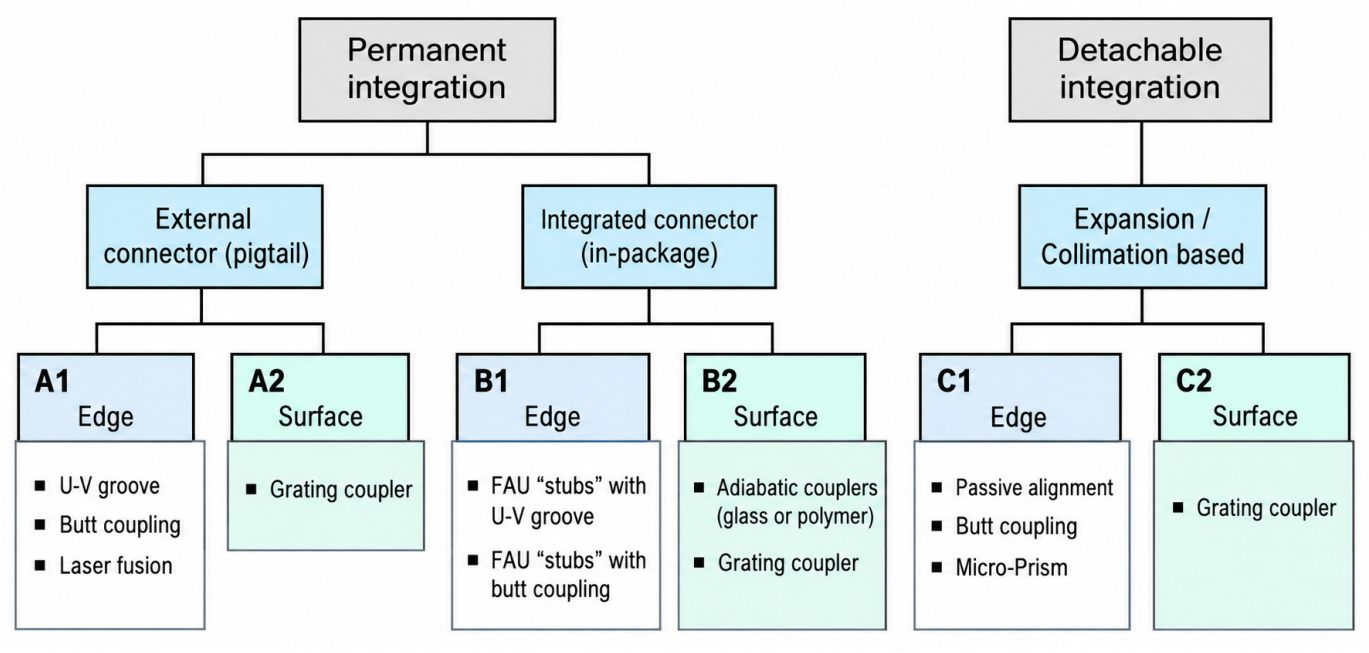

Figure 5 – Categorization Tree

The six categories above (A1-C2) are designated for easier reference into the following sections.

Permanent vs. Detachable Integration

A permanent integration approach shall consist of the attachment of optical components to the photonic package in a manner that does not allow subsequent removal or replacement without damage to the assembly. The integrated optical component shall be capable of withstanding all downstream manufacturing processes, including but not limited to printed circuit board (PCB) reflow, cleaning operations, and environmental reliability testing.

In contrast, a detachable integration implies that most of the fixturing for light transfer to a fiber ribbon array can be removed and does not have to withstand reflow or other manufacturing processes. However, some permanent feature such as a lens array must still be included within the PIC for light beam expansion and collimation.

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External vs. Integrated Connector for Permanent Integration

External connectors shall consist of the permanent attachment of an optical subassembly, and their main component is a pigtail fiber ribbon that is typically several centimeters in length. A pigtail fiber has a standard connector on one end and is exposed as bare fiber on the other end for the permanent attach to a module.

The Fiber Array Unit (FAU) assembly shall typically include the following elements:

- A standardized optical connector interface such as MPO, MT, FC (IEC standard) enabling mating with industry-standard fiber-optic cables
- A ribbon or bundled fiber segment of defined length typically of several centimeters
- A permanent coupling interface at the FAU tip, designed to interface with the PIC die on the edge or the surface.

This configuration shall be referred to as pigtail integration. In this configuration, the optical connector shall remain external to the device package and the fiber assembly beyond the final attachment point shall be considered mechanically free. This implies that handling of a module for a manufacturing process typically requires a physical support to hold the fiber ribbon and avoid damage to the connector interface.

For an integrated connector, on the other hand, a standard optical connector interface shall be integrated in the package, typically glued to a lid or a substrate. A fiber stub, short piece of optical fiber inside a ceramic of metal tube, may be used for this kind of connection and does not require supplementary physical support for module handling. The external fiber connection is close to a module (~cm).

The attachment of the FAU to the PIC die shall be achieved using one or more of the following methods:

- Adhesive bonding (e.g., epoxy), which shall be considered the current baseline method
- Laser-assisted fusion bonding
- Anodic bonding

Some geometrical constraints are inherent to each approach and will be defined and established into the part. The final mechanical interface between the FAU and the package shall incorporate a strain relief structure to ensure mechanical robustness and to protect optical alignment from stress induced by handling, vibration, or cable movement.

Strain relief implementations may include:

- Adhesive-based fixation (e.g., epoxy bonding)
- Mechanical retention features (e.g., clamps, boots, overmolded structures)

An example of adhesive-based fixation with strain relief is shown in Figure 6.

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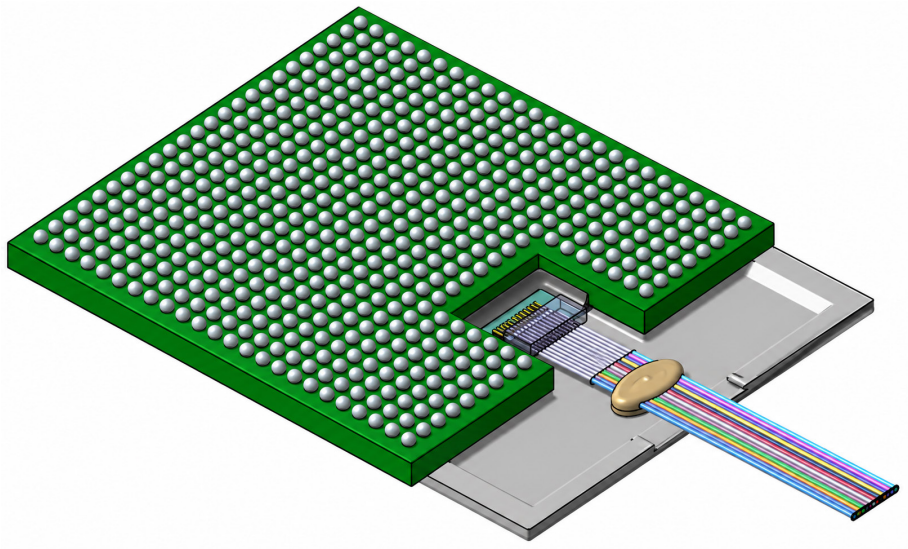

Figure 6 – Example of a Fiber Array Unit with Strain Relief (A1)

2.2.1. Edge Coupling

In the case of edge coupling with a pigtail connector (A1), when the optical coupling interface is located on the edge of the PIC die, permanent FAU integration shall be implemented using one or more of the following approaches:

- **Butt coupling**: The FAU is integrated directly on the waveguide (WG) / taper facet and shall typically incorporate a glass block to maintain defined spacing (pitch) between fibers and to facilitate handling during assembly. The interface facet of the glass block shall be polished and may incorporate additional structures such as lensed interfaces or mode-matching elements. During assembly, the FAU shall be aligned relative to the PIC die using active alignment techniques. Alignment optimization shall be performed using electrical or optical feedback to maximize coupling efficiency.

- **Self-aligned coupling:** The FAU is integrated directly on some self-alignment structures etched directly into or close to the coupling interface on the PIC die. These structures shall be (but not limited to) V-grooves or U-grooves respectively etched using isotropic and anisotropic methods. The FAU shall typically incorporate a bare fiber section to fit into the alignment structures. The fiber tips shall be mechanically, or laser cleaved or shall include lensed interfaces or mode-matching elements. During assembly, the FAU shall be coarsely aligned since the self- alignment structure takes care or the fine alignment with the optical facet on the PIC die.

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2.2.2. Surface Coupling

An alternative configuration for light coupling between a FAU and a PIC is to realize an interface so that the optical path is at the surface of the die instead of the edge. This category presents the advantage of being compatible with wafer-level testing, as dicing is not required. However, some design rules are required to allow for sufficient area and beach front for coupling on the PIC surface.

One approach for surface coupling involves the design and fabrication of a waveguide array in a material for which the index contrast is such that the core size is between that of a single mode glass FAU and that of a SiN or Si waveguides. Typically, this intermediate medium is made of glass or polymer and integrates pitch conversion to save real estate on a PIC. Light from an FAU is coupled by the edge of the glass or polymer piece, and light transfer in a PIC is achieved by evanescent coupling, placing the cores very close to those of the PIC.

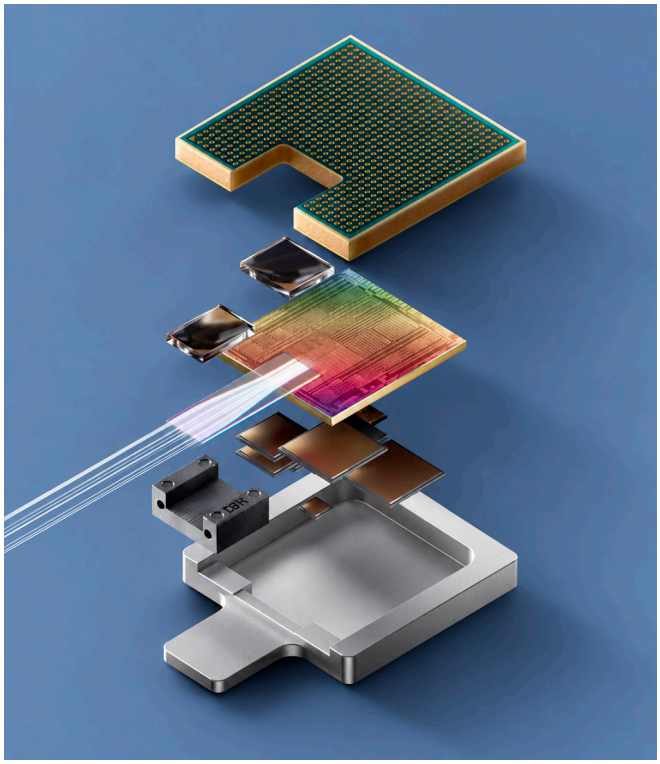

Figure 7 – Example of a Polymer Waveguide Surface Coupled Module with Integrated Connector (B2) [IBM Newsroom]

Another method consists in the inclusion of a diffraction grating pattern within the PIC to induce a momentum transfer from an in-plane geometry to an out-of-plane geometry. When light from a glass fiber reaches the grating at a specific angle of incidence, it is coupled horizontally to a photonic waveguide. Typically, this physical mechanism is polarization-dependent. There are requirements for the design and assembly of grating couplers.

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2.3. Design Rules and Definitions for Optical Attach

Regardless of the attach mechanism, a PIC designer must follow a set of ground rules to ensure compatibility with packaging requirements. Figure 8 illustrates some of the parameters that shall be specified by the OSAT.

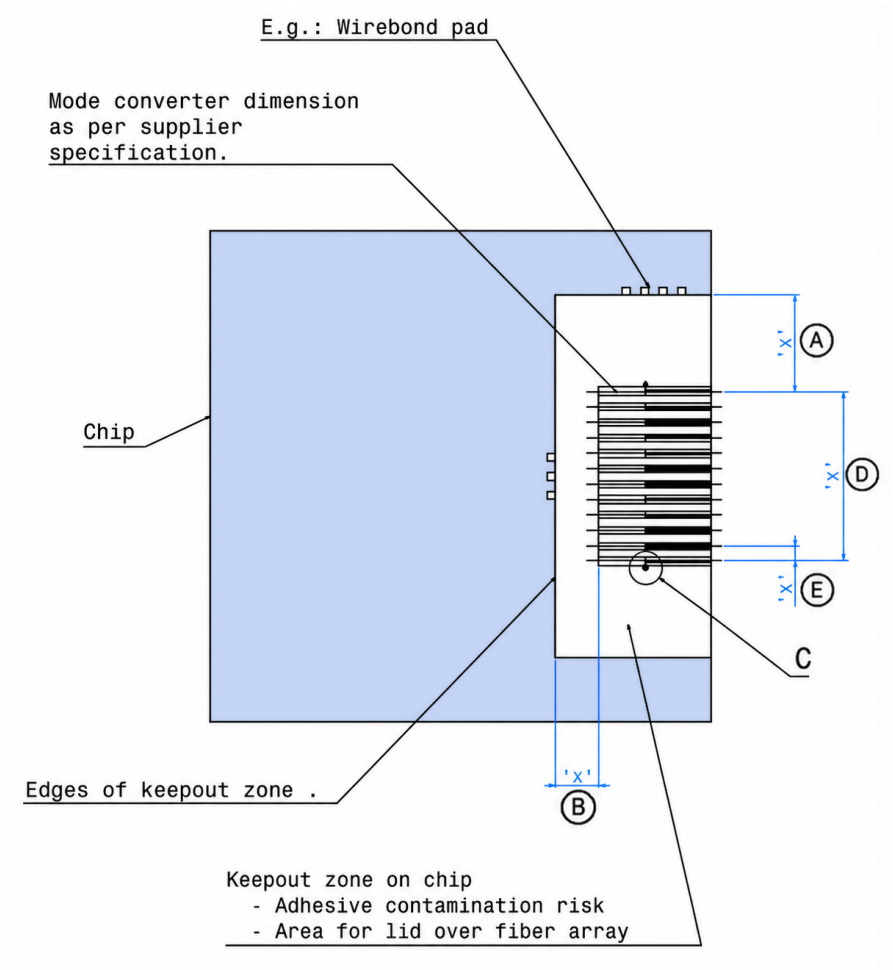

Figure 8 – Illustration of Nominal Ground Rules for Packaging Considerations

A	Keepout zone – Distance from edge of exterior groove
B	Keepout zone – Distance from end of attach region
C	Fiducial cross line size
D	Core pitch
E	Fiber pitch in the case of single fiber attach
L	Lengh of pigtail fiber or other waveguide material to attach (not shown)

Table 1 – Explanation of Clearance Parameters in Figure 7

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There is a need to standardize connectors and the length of optical components attached to save costs, as well as all other design parameters to the PIC could be compatible with multiple attachment schemes.

Reflow compatibility: When a statement is made about reflow compatibility for an attach mechanism, the manufacturer shall specify the temperature cycle, the number of cycles that the assembly can tolerate, as well as the maximum allowed optical loss variation after thermal stress.

Cleanliness: The environment in which optical components are allowed to sit or be carried before and after assembly shall be specified and followed by the OSAT and component makers. The maximum level of contamination on optical surfaces shall be defined with an appropriate quantitative characterization method.

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3. Design Simulation and Modeling

Silicon Photonics manufacturing relies on a seamless design, simulation and modeling workflow which predicts the technical behavior of the future manufactured Photonic Integrated Circuit based device. To establish an open ecosystem being able to contribute to the different stages of this workflow, alignment is required on general parameter definitions such as the naming convention, the maturity level of components available in Process Design Kit (PDK) of foundries and the port convention of PIC building blocks and sub-systems.

This section is organized as follows: A general parameter definitions section is first provided, followed by a dedicated section on design parameters relevant for fiber-to-chip coupling and a proposed file format for data exchange between simulation tools involved in the design of fiber-to-chip coupling systems. These latter sections are introduced to standardize the workflow for fiber-to-chip coupling system design.

3.1 General Parameter Definitions

In order for the user to be able to compare the types and attributes (optical bands, polarization, maturity, etc.) of PIC building blocks and PIC sub-systems of different foundries PDKs or IP providers it is of utmost importance to use the same naming convention. The following naming convention for PIC cells shall be used throughout the document.

provider_cellname_opticalband_polarization_version_maturity

- opticalband -> Operation band: oband, cband, clband
- polarization -> Polarization mode: te, tm. For polarization multiplexers (PC, MDM, PSR) the mode is not precise.
- maturity -> Maturity level: m0, m1 or m2, m3 (see paragraph below)

It is important to know the maturity level of PIC building blocks and sub-systems in PDKs of foundries in order to provide the technical behavior in a sufficient and acceptable accuracy. The maturity level of building blocks refers to the development stage of the device, indicating its level of reliability, stability, and completeness of the information offered to the users.

The maturity level may be defined in the end of the name of the cells in PDKs of foundries, so that users can recognize the maturity stage of the cell immediately.

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- **m0 = Concept/Simulated:** Blocks based on theory and physical simulations (optical/electromagnetic), but not yet manufactured or validated
- **m1 = Fabricated/Preliminarily Tested (Prototype):** The component has been manufactured in a test batch (Multi-Project Wafer - MPW) and measured.
- **m2 = Validated/Calibrated (PDK Release):** Statistical die to die specifications available at least from one manufacturing run. The block is officially offered in the foundry's Process Design Kit (PDK). It features an empirically validated compact model, guaranteeing its behavior in circuit simulations.
- **m3= Automation Support (Production PDK):** Qualified die to die, and lot to lot through several runs. The blocks fully comply with Design Rule Checking (DRC), support automatic routing, and are integrated into Electronic/Photonic Design Automation (EPDA) tools.

To facilitate the use of PDK libraries from different foundries and EDA tools, the following port convention shall be used: When S-matrices are discussed, the term S nmji corresponds to the S parameter with output mode n, input mode m, output port j, input port i. When only one mode is used (TE 0 generally), these terms can be reduced to S ij. The ports are numbered following a common convention: from north to south, starting with the west side and then east side, as illustrated Figure 9. The modes are numbered alternating between TE and TM : TE 0 , TM 0 , TE 1 , TM 1 etc. For example, the west and east ports will be respectively named optXin and optXout where X is the index increasing from north to south when more than one port is present (optin, opt2in).

Figure 9 – Port Number Convention

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Simulating and modeling PIC based devices requires also a standardized way of representing data. This enables an open ecosystem to be comparable and interoperable. This particularly pertains to comparing test results with simulated performance and vice versa. Experimental characterization might result in outliers that are not representative of the actual behavior of the device. In order to filter out these extreme outliers, the Interquartile Range (IQR) method shall be used. It filters out the measurements that lie outside 1.5 times the IQR from the quartiles Q1 and Q3, defined as the 25th and 75th quartile of the distribution of the measurements. The interquartile range is defined as the difference between these quartiles.

$$IQR = Q\,3 - Q1$$

$$\text{Lower bound} = Q\,1 - 1.5 \cdot IQR$$

$$\text{Upper bound} = Q\,3 + 1.5 \cdot IQR$$

Depending on the purpose of the component, either the value at the target wavelength or the average over the available wavelength range is considered for this method. This latter approach is typically used for broadband components. Other important metrics for result plots are the Lower Specification Limit (LSL), Target and Upper Specification Limit (USL). In addition to the plots, the specifications are summarized in a metrics table which uses the Lower Specification Limit (LSL), Target and Upper Specification Limit (USL) to give an overview. These values are derived from the statistical distribution of the measured data.
The lower and upper specification limits are defined as 3 standard deviations σ from the mean.

$$\text{Target} = \mu$$

$$LSL = \mu - 3 \cdot \sigma$$

$$USL = \mu + 3 \cdot \sigma$$

Other data required may include footprint (device size) and temperature specifications.

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General Parameter Definitions

Parameter	Definition	Ref Code	Units	Formula
Center Wavelength	Peak in1 → out2 closest to wavelength of operation	[CW]		max S31
Operation Band	C, L, or O band	[OB]		
Channel Spacing	Wavelength difference between two channels	[CS]		|λ c,2→i – λc,2→i±1|
Crosstalk	Power difference between on- and max off-channel at λ c	[XT]		max i ¹3 –10 log10 (|S31|2/ |Si1|2) λ=λc
Conversion loss	Losses of power measured at port out2 when injecting TE 1 in port in1	[CVL]		CL = –10 log 10 | S1331|2
Crosstalk TE0	Fraction of power measured at port out2 compared to port out1 upon injecting TE0 in port in1	[XT TE0]		XT TE 0 = 10 log 10 |S1121|2/ |S1131|2
Crosstalk TE1	Fraction of power measured at port out1 compared to port out2 upon injecting TE 1 in port in1	[XT TE1]		XT TE 1 = 10 log 10 |S1331|2/ |S1321|2
Intra-wafer spectral shift	Deviation center wavelength of each reticle from wafer averaged	[IWSS]		Δλ i = λ i – λc

Table 2 – General Parameter Definitions

3.2. Parameter Definitions for Fiber-to-Chip Interface

This section is used to establish a common definition for the critical parameters needed in the design of the fiber-to-chip coupling interfaces for optical interconnects used in silicon photonics devices. This standard shall provide a consistent set of definitions to ensure that:

- All members of the ecosystem involved in the design and manufacture of fiber-to-chip coupling interfaces are measuring and quantifying the performance of their systems in a standard manner. This shall ensure that members of the ecosystem who wish to integrate third-party fiber-to-chip coupling systems into their larger devices have a standard method to compare the performance of systems offered from multiple vendors.
- All design tools used to model fiber-to-chip coupling interfaces characterize the performance of these systems using equivalent metrics and that the tools report data and provide results in a consistent manner based on these standard definitions. This shall ensure that engineers have a standard method to compare the performance of various designs for their systems across multiple simulation solutions.

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This standard shall not impose a prescription for a preferred design architecture. Different design architectures may be considered in the development of fiber-to-chip coupling interfaces to ensure that the most cost-effective solutions are identified, and that these solutions can be manufactured robustly at scale. The use of common definitions in the design of fiber-to-chip coupling interfaces ensures that different solutions are being compared with standardized methods.

3.2.1 Parameter Definitions

The data below is provided in a consistent structured format comprised of:

- **Parameter Name** - how the parameter should be referenced
- **Definition** - what the parameter measures
- **Units** - the units of measurement for the parameter
- **Degrees of Freedom** - the relevant system inputs that can influence the parameter measurement
- **Reference Condition** - the nominal values for the system inputs at which the parameter is measured
- **Reporting and Statistical Reporting** - how results shall be presented with variability and yield metrics. Statistical reporting (μ, σ, yield) shall be included whenever multiple devices are measured or process variation is assessed.

Parameter Definitions for Fiber-to-Chip Coupling System Design -

Parameter	Definition	Ref Code	Units	Degrees of Freedom	Reference condition	Measurement Methods	Reporting
Coupling Loss	The loss of optical power that occurs when light travels from the fiber into the chip (or vice versa) due to the presence of the coupler or connector. This includes the Insertion Loss, the Return Loss, and the Polarization Dependent Loss.	[CL]	dB	Wavelengths (l), temperature (T), alignment (x,y,z,θx,θy), polarization (TE/TM)	Ref λs, 25°C, optimal alignment, specified polarization (TE/TM)	1. Direct Transmission with References (Substitution Method) 2. Cutback Method 3. Optical Time Domain Reflectometry (OTDR) 4. Optical Frequency Domain Reflectrometry (OFDR) 5. Spectral Characterization with Broadband Source 6. Back-Coupling or End-Facet Monitoring	Loss (dB) at ref condition; loss vs. λ; loss vs. T

Table 3 – Parameter Definitions for Fiber-to-Chip Coupling System Design

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Parameter Definitions for Fiber-to-Chip Coupling System Design - (con't)

Parameter	Definition	Ref Code	Units	Degrees of Freedom	Reference condition	Measurement Methods	Reporting
Insertion Loss	The optical power loss at the interface where light transitions from the optical fiber into the onchip waveguide (or vice versa). It encompasses all mechanisms that reduce transmitted power, including: - **Mode-Mismatch Loss** - **Geometric Misalignment** - **Impedance-Mismatch & Fresnel Reflections** - **Longitudinal Loss** - **Surface Quality & Scattering & Absorption** - **Packaging & Thermal Stress** The Insertion Loss represents the maximum power loss that can be measured.	[IL]	dB	Wavelength (l), temperature (T), alignment (x,y,z,θx,θy), polarization (TE/TM)	Ref λ, 25°C, optimal alignment, specified polarization (TE/TM)	1. **Direct Measurement with Light Source and Optical Power Meter** 2. **Optical Time Domain Reflectometry (OTDR)** 3. **Optical Frequency Domain Reflectrometry (OFDR)** 4. **Cutback Method** 5. **Interferometric Methods**	Loss (dB) at ref condition; loss vs. λ; loss vs. T
Internal Return Loss	The amount of optical power reflected back toward the source (laser) due to impedance mismatch or refractive index discontinuities at the coupling interface. This is a measure of loss within the chip itself.	[IRL]	dB	Wavelength (l), temperature (T), alignment (x,y,z,θx,θy), polarization (TE/TM)	Ref λ, 25°C, optimal alignment, specified polarization (TE/TM)	1. **Simulation setup**	Loss (dB) at ref condition; loss vs. λ; loss vs. T
External Return Loss	The amount of optical power reflected back toward the source (laser) due to impedance mismatch or refractive index discontinuities at the coupling interface, as measured by an probe or external measurement device (as seen from outside the chip).	[ERL]	dB	Wavelength (l), temperature (T), alignment (x,y,z,θx,θy), polarization (TE/TM)	Ref λ, 25°C, optimal alignment, specified polarization (TE/TM)	1. **Continuous Wave Reflectometry (OCWR)** 2. **Optical Frequency Domain Reflectometry (OFDR)**	Loss (dB) at ref condition; loss vs. λ; loss vs. T

Table 4 – Parameter Definitions for Fiber-to-Chip Coupling System Design (con't)

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Parameter Definitions for Fiber-to-Chip Coupling System Design - (con't)

Parameter	Definition	Ref Code	Units	Degrees of Freedom	Reference condition	Measurement Methods	Reporting
Crosstalk	The amount of optical power leaked from one channel into adjacent one within a multi-channel device. This may become important with smaller pitch size and higher density.	[XTCTK]	dB	Wavelength (l), channel spacing, number of adjacent channels, polarization (TE/TM)	Ref λ, 25°C, one channel illuminated	1. **Direct Measurement with Light Source and Optical Power Meter**	Nearest and next-nearest neighbor coupling (dB); coupling vs. λ; coupling vs. pitch
Polarization Dependent Loss	The difference between the peak and minimum coupling efficiencies (the minimum and maximum coupling loss) measured across all input polarization states.	[PDL]	dB	Wavelength (l), temperature (T), input polarization	Ref λ, 25°C, optimal alignment	1. **Polarization-Scanning Method** 2. **Mueller-Matrix (Four-State) Method**	Loss (dB) at ref l; PDL vs. l
Optical Bandwidth	The range of wavelengths over which the coupling loss stays within 1 dB of the peak performance.	[OBW]	nm	Center wavelength (l), temperature (T), input polarization	25°C, optimal alignment, specified polarization	1. **Tunable Laser + Optical Power Meter** 2. **Broadband Source + Optical Spectrum Analyzer** 3. **Cutback Method for Cascaded Structures**	1-dB bandwidth (nm); loss vs. l curve; Dl/DT
Polarization State	The polarization state of the beam that travels through the fiber or waveguide. May be any state (TE, TM, or mixed), once defined this state needs to be maintained throughout the entire link.	[PS]		Fiber type, waveguide geometry, coupling architecture	Ref λ, specified fiber type	1. Polarization Meter 2. Light Source + Polarization Controller + Optical Power Meter	Polarization (TE/TM) at input/output; PER (dB)
Mode Field	The Mode Field Diameter (MFD) of the beam that travels through the fiber or waveguide. This is symbolically referred to as D4s, and is calculated as 4 x s, where s is the standard deviation of the intensity distribution in the transverse direction. The exact calculation of D4s is given in ISO standard 11146 (https://www.iso.org/obp/ui/en/#iso:std:iso:11146:-1:ed-2:v1:en)	[MF]	mm	Wavelength (l), polarization, transverse axes	Measured right at the fiber or waveguide facet	1. Near-Field Imaging 2. Far-Field (Angular) Scanning 3. Scanning-Edge / Knife-Edge Technique	MFD_x, MFD_y (mm); MFD (mm) vs. l; mode area.

Table 4 – Parameter Definitions for Fiber-to-Chip Coupling System Design (con't)

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Parameter Definitions for Fiber-to-Chip Coupling System Design - (con't)

Parameter	Definition	Ref Code	Units	Degrees of Freedom	Reference condition	Measurement Methods	Reporting
Fiber Cleave Angle	A measure of how much the end-face, or tip, of the optical fiber is cut away from being perfectly perpendicular to the fiber axis.	[FCA]	Degrees	N/A	Measured vs. fiber axis	1. Based on manufacturer specification	Angle ±Dq
Fiber Pitch Size	The spacing between the mode field centers of adjacent optical fibers in an array.	[FPS]	mm	Array manufacturing tolerance, thermal expansion	25°C, measured at fiber array endface	1. Optical Profilometry 2. Scanning Electron Microscopy (SEM 3. Optical Microscopy with Calibration 4. Laser Scanning Microscopy	Nominal pitch ±Dp; uniformity across array
Fiber Absolute Position Deviation	The RMS deviation of fiber position from a uniform grid. This is calculated using the deviation of each fiber from its "ideal" position (Δxi = xi - xideal and Δyi = yi - yideal) to generate an RMS sum: ∑ (i = 1 to N) Δxi2 +Δyi2. The calculation of the deviation includes the fiber cladding.	[FAPD]	mm	Lateral position (x,y) per fiber, substrate tolerance	25°C; ideal grid from nominal pitch	1. Interferometric Fringe Pattern Analysis 2. Machine-Vision & CCD-Based Profiling 3. Active "Dithering" & Feedback Throughput Optimization 4. Profilometry & Microlens Array Mapping	RMS (mm); per-fiber offset map; max single-fiber deviation
Coupling Region	The region over which the fiber mode is converted to the on-chip waveguide mode (or vice versa). This includes tapered sections on both the fiber (e.g., a thin tapered tip) and the chip (e.g., an inverse or multi-tip tapered waveguide). It also includes the cladding or cap layers around the tapered region (higher-index caps, polymer waveguides, etc.) that help confine and direct light into the chip interface. In packaged or array-coupled devices, the coupling region also includes mechanical-aligning structures (such as V-grooves or etched facets) that guide and stabilize the fiber position relative to the chip-coupling feature.	[CR]	mm	Taper geometry (fiber & chip), cladding/cap properties, alignment structures	N/A	1. Physical Characterization 2. Optical Characterization	Total footprint

Table 4 – Parameter Definitions for Fiber-to-Chip Coupling System Design (con't)

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Parameter Definitions for Fiber-to-Chip Coupling System Design - (con't)

Parameter	Definition	Ref Code	Units	Degrees of Freedom	Reference condition	Measurement Methods	Reporting
Alignment Tolerance	The 3D region on the chip surface in which the Coupling Loss stays within 0.5 dB of peak performance. This region is relative to the location of the peak intensity of the optical beam at the chip surface, and encompasses both lateral and angular shift of the beam relative to the location of the peak intensity.	[ALT]		Alignment (x,y,z,θx,θy)	Peak coupling alignment		±Dx, ±Dy, ±Dz, ±Dq for 1-dB loss change
Beam Angle	The orientation of the optical beam relative to the chip surface normal.	[BA]		In-plane (θx), out-of-plane (θy), l dependence	Optimal alignment, ref l, 25°C	1. **Maximize Coupled Power via Angular Scanning** 2. **Beam Profiling** 3. **Interferometric or Fringe-Based Angle Detection** 4. **Active Alignment with Optical Intensity/Polarization Feedback**	Nominal angle ±Dq; angular BW for 1-dB loss change; angle vs. l
Coupler Pitch Size	The center-to-center spacing between adjacent coupling features on the photonic integrated circuit (PIC), such as grating couplers or waveguide arrays.	[CPS]		Manufacturing tolerance	As-designed layout	1. **Optical Profilometry** 2. **Scanning Electron Microscopy (SEM)** 3. **Optical Microscopy with Calibration** **Laser Scanning Microscopy**	Nominal pitch; uniformity; mismatch vs. fiber pitch
Beachfront Density	The number of optical fibers that can be connected to the edge or onto the surface of a photonic integrated circuit (PIC) within a given area.	[BFD]		Manufacturing tolerance	As-designed layout	1. **Count the number of optical interfaces; Measure the edge length where coupling occurs; Calculate from the ratio**	Interfaces per unit length or area; effective pitch; total count and footprint

Table 4 – Parameter Definitions for Fiber-to-Chip Coupling System Design (con't)

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3.2.2 Summary Table of Reference Codes for Parameter Definitions

Parameter	Reference Code
Coupling Loss	[CL]
Insertion Loss	[IL]
Internal Return Loss	[IRL]
External Return Loss	[ERL]
Crosstalk	[XT]
Polarization Dependent Loss	[PDL]
Optical Bandwidth	[OBW]
Polarization State	[PS]
Mode Field	[MF]
Fiber Cleave Angle	[FCA]
Fiber Pitch Size	[FPS]
Fiber Absolute Position Deviation	[FAPD]
Coupling Region	[CR]
Alignment Tolerance	[AT]
Beam Angle	[BA]
Coupler Pitch Size	[CPS]
Beachfront Density	[BFD]

Table 4 – Summary of Table Reference Codes for Fiber-to-Chip Coupling System Design

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3.2.3 Typical Design Values for Parameters

Category	Reference Code	Target Specifications	Notes
Performance	[CL]	≤1.5 dB (high-perf); ≤3.0 dB (standard)	
	[IL]	≤1.0 dB (high-perf); ≤2.0 dB (standard)	Max power loss measured, including impact of polarization
	[IRL]	≥20 dB	
	[ERL]	≥20 dB; ≥30 dB for laser-sensitive	
	[XT]	≤–30 dB	
	[PDL]	≤0.5 dB (pol-insensitive apps)	
Optical	[OBW]	≥30 nm (C-band); ≥80 nm (broadband)	
	[PS]	PER ≥20 dB (PM systems)	
	[MF]	9.2 µm +- 0.2 µm for SMF	
	[BA]	Manufacturer dependent	
Physical	[FCA]	Manufacturer dependent (common: 0° +- 0.3° or 8°)	
	[FPS]	Per design (common: 127 or 250 µm)	
	[FAPD]	≤0.5 µm RMS (high-precision)	
	[CR]	Design-dependent	
	[AT]	ΔL ≤0.5 dB from peak	
	[CPS]	Manufacturer dependent	
	[BFD]	Manufacturer dependent	
Crosstalk	[XT]		Adjacent and non-adjacent isolation of wavelengths > 30 dB / 40 dB respectively

Table 5 – Nominal Values for Parameters used in Fiber-to-Chip Coupling Design

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3.2.4 Schematic Layout Examples of Fiber-to-Chip Coupling Configurations

3.2.4.1 Vertical Coupling with Single Core Fiber

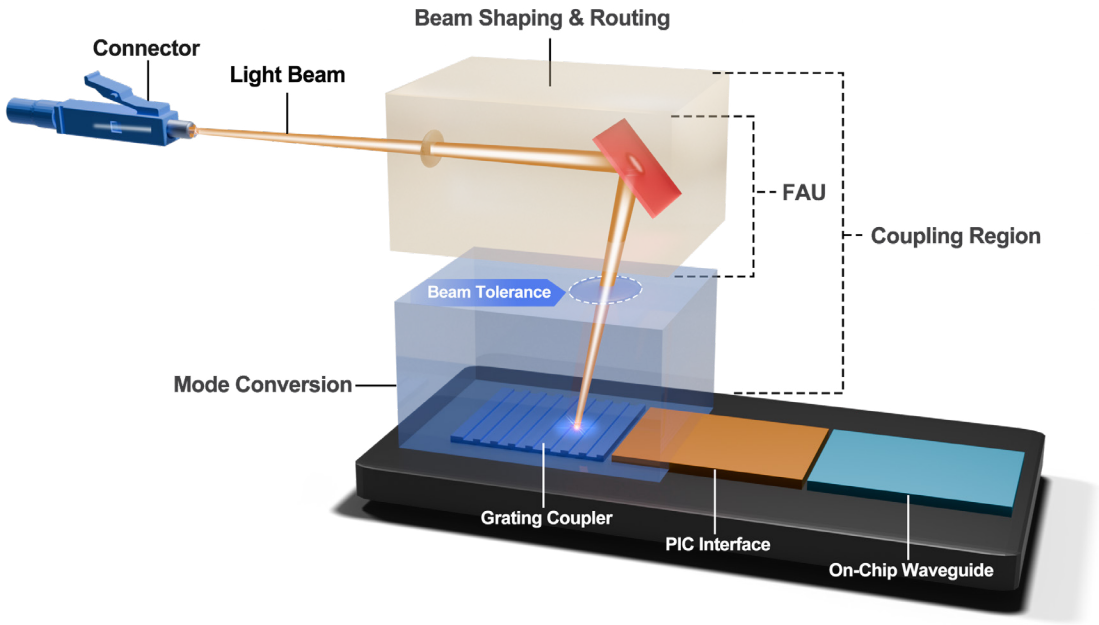

Figure 10 – Vertical Coupling with Single Core Fiber

3.2.4.2 Vertical Coupling: Single Core Fiber with Polarization

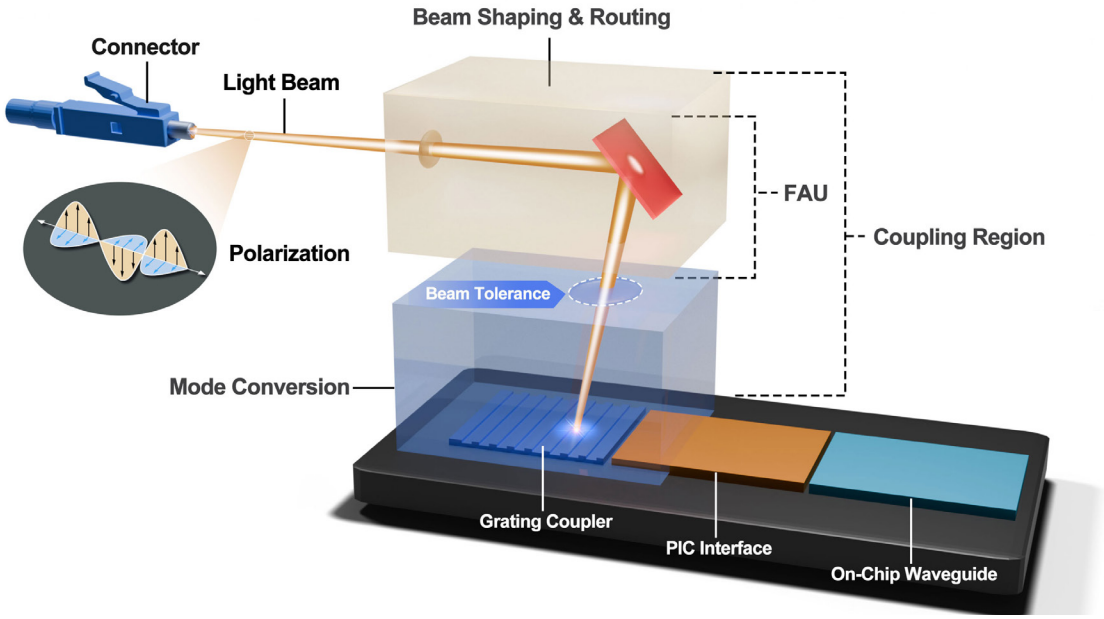

Figure 11 – Vertical Coupling with Single Core Fiber showing Polarization

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3.2.4.3 Vertical Coupling with Multicore Fiber

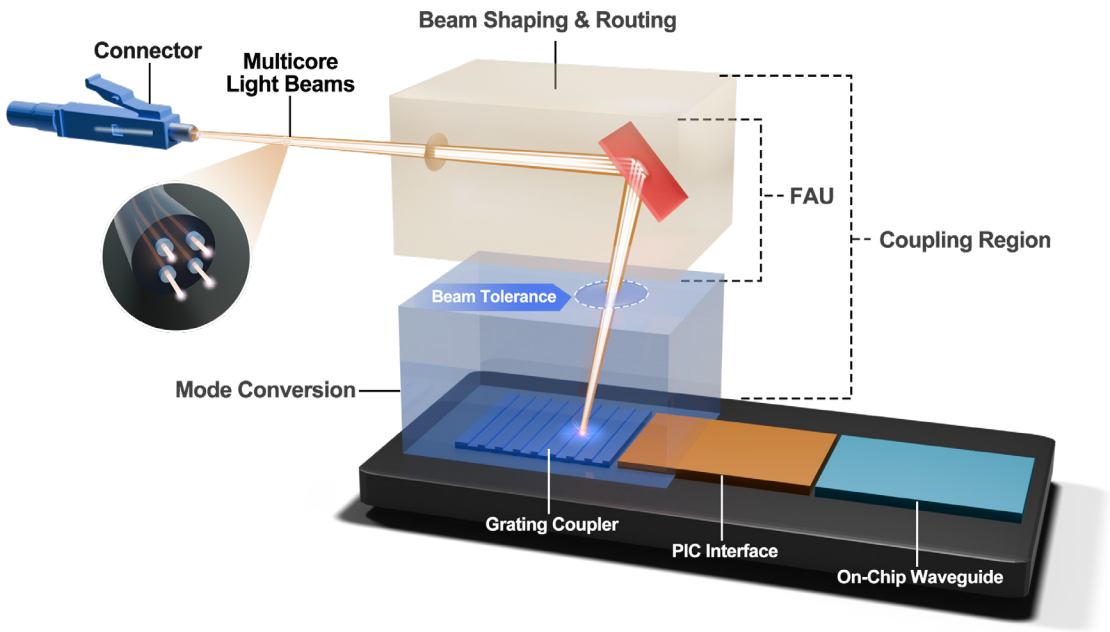

Figure 12 – Vertical Coupling with Multicore Fiber

3.2.4.4 TSMC COUPE™ Architecture

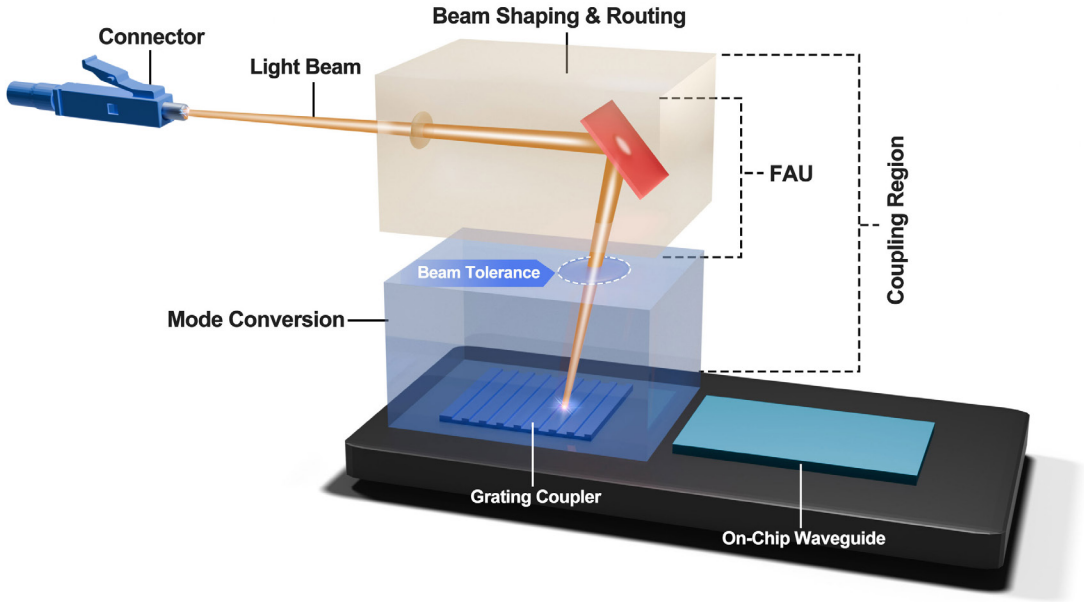

Figure 13 – TSMC COUPE Architecture

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3.2.4.5 Edge Coupling with Multicore Fiber

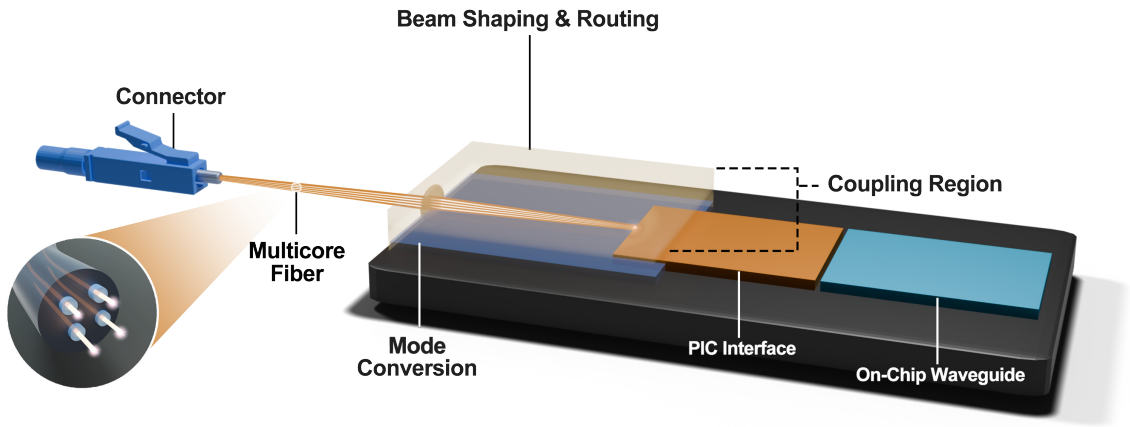

Figure 14 – Edge Coupling with Multicore Fiber

3.3 Standard for Data Exchange between Modeling Tools used for Fiber-to-Chip Interface

This section is used to establish a common file format for interoperability between the macroscale and microscale modeling tools used in the design of the fiber-to-chip coupling interfaces for optical interconnects used in silicon photonics devices. In this section we aim to provide a common set of requirements for the data that is exchanged between tools and the syntax of the file in which that data is stored, to ensure that:

- All members of the ecosystem involved in the design and manufacture of fiber-to-chip coupling interfaces can use a standard method for interoperability between their macroscale and microscale modeling tools. This will ensure that members of the ecosystem can work together in a robust and seamless manner regardless of which modeling tools any member may be using.
- All design tools used to model fiber-to-chip coupling interfaces can work together to exchange data without the need for error-prone data translation or modification. This will ensure that engineers have a fair and neutral way to compare the performance of various designs for their systems across multiple modeling solutions.

3.3.1 File Definition

The Open Ansys Zemax Beam File (ZBF) format will serve as the template for interoperability between macroscale and microscale modeling tools used in the design of the fiber-to-chip coupling interfaces. While the ZBF file supports both a human-readable ASCII format as well as a binary format, this version of the standard will only support the ASCII format for ease of use.

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3.3.1.1 ASCII Format

The first line must be the single character "A", followed by the other data values specified.

A: indicates a text file.

version: The format version number, currently 1.

nx: The number of x samples.

ny: The number of y samples.

ispol: The "is polarized" flag; 0 for unpolarized, 1 for polarized.

units: 0 for mm, 1 for cm, 2 for in, 3 for meters.

unused 1: Currently unused, may be any value.

unused 2: Currently unused, may be any value.

unused 3: Currently unused, may be any value.

unused 4: Currently unused, may be any value.

dx: The x direction spacing between points.

dy: The y direction spacing between points.

zx: The z position relative to the pilot beam waist, x direction.

Rx: The Rayleigh distance for the pilot beam, x direction.

wx: The waist in lens units of the pilot beam, x direction.

zy: The z position relative to the pilot beam waist, y direction.

Ry: The Rayleigh distance for the pilot beam, y direction.

wy: The waist in lens units of the pilot beam, y direction.

lambda: The wavelength in lens units of the beam in the current medium.

index: The index of refraction in the current medium.

re: The receiver efficiency. Zero if fiber coupling is not computed.

se: The system efficiency. Zero if fiber coupling is not computed.

unused 1: Currently unused, may be any value.

unused 2: Currently unused, may be any value.

unused 3: Currently unused, may be any value.

unused 4: Currently unused, may be any value.

unused 5: Currently unused, may be any value.

unused 6: Currently unused, may be any value.

unused 7: Currently unused, may be any value.

unused 8: Currently unused, may be any value.

Ex real value for point 1

Ex imaginary value for point 1

Ex real value for point 2

Ex imaginary value for point 2

etc... for 2*nx*ny Ex values.

If polarized, followed by 2*nx*ny Ey values.

The Ex and Ey values are defined such that the Ex*Ex + Ey*Ey is in units of watts.

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Thank you

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