Consortium For On-Board Optics

COBO 8-Lane & 16-Lane On-Board Optics Specification

Release 1.1

This specification defines the characteristics of 8 and 16 lane On-Board Optics (OBO) for use in up to 1x 400G and 2x 400G applications and provides a common specification for systems manufacturers, system integrators, component manufacturers, and suppliers of on-board optics.

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Table of Contents

Table of Contents (Cont')

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Figures

Figures (Con't)

Tables

Terms and Defintions

Bank	For the 16-lane OBO, a collection of 8 electrical lanes and its corresponding optical lanes
C2M	Chip to Module
CDR	Clock and Data Recovery
CMIS	Common Management Interface Specification
CML	Current Mode Logic
COBO	Consortium for On-Board Optics
Connectorized Module	a PMD with a separable fiber optic connection on the module itself (see also Receptacled module)
Data Center Cabling	The IEEE defined copper or fiber optic infrastructure between the two MDI points
Dual LC	Dual Lucent Connector
Egress	Datapath from Host to Media
FFU	For Future Use
GPIO	General Purpose Input Output
HS	High-Speed
IEEE	Institute of Electrical and Electronics Engineers – The IEEE802.3 organization develops standards for Ethernet including the electrical and optical interfaces
Ingress	Datapath from Media to Host
LS	Low-Speed
LVCMOS	Low Voltage CMOS complementary metal oxide semiconductor
LVTTL	Low voltage TTL transistor logic
MDI	Medium Dependent Interface – the IEEE defined link location at which the copper or fiber optic connector mates to the PMD
MPO	Multi-fiber Push-On - Physical contact connector with multiple fibers arranged in a linear array of up two rows. Available in up to twelve fibers per row.
MPO-16	Multi-fiber Push-On - Available in up to sixteen fibers per row and up to two rows. Keyed differently to prevent mating with MPO.
MPO-12	MPO connector with 12 fibers
MR	Medium Reach – An electrical interface capable of supporting ~20dB loss at a frequency of baud rate/2
OBO	On-Board Optics – an optical transmitter, receiver, or transceiver which is mounted to the interior of the PCBA
OIF	Optical Internetworking Forum – Develops electrical and optical interoperability agreements

Terms and Defintions (Con't)

PMD	Physical Medium Dependent – the IEEE defined transceiver module minus any copper or fiber optic cabling necessary to take the signal to the card edge
Pigtailed Module	A PMD with an inseparable length of fiber, typically terminated with a fiber optic connector, exiting the module and routing to the card edge
Pluggable Optical Module	An optical transmitter, receiver, or transceiver which gets mounted to the edge of the PCBA
PCBA	Printed Circuit Board Assembly – the printed circuit board along with all the typical components (resistors, capacitors, etc.) soldered in place
Receptacled Module	A PMD with a separable fiber optic connection on the module itself (see also Connectorized module)
RU	Rack Unit – A unit of measure describes the height of electronic equipment designed to mount in a 19-inch rack or a 23-inch rack and is 1.75 inches (44.45mm) high
TP2	Test Point 2 - The IEEE defined location at which optical power is measured from the source PMD
TP3	Test Point 3 - The IEEE defined location at which optical receive signal is measured going to the destination PMD
TWI	Two wire interface used for management interface
VSR	Very Short Reach – An electrical interface capable of supporting a ~10dB loss at a frequency of baud rate/2

References

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2. ANSI-TIA-604-18, FOCIS 18 - Fiber Optic Connector Intermateability Standard - Type MPO- 16
3. IEC 61754-7-1, Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 7-1: Type MPO connector family - One fibre row (similar to FOCIS 5)
4. IEC 61754-7-2, Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 7-2: Type MPO connector family - Two fibre rows (similar to FOCIS 5)
5. IEC 61754-7-3, Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 7-3: Type MPO connector family - Two fibre rows
6. IEC 61754-7-4, Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 7-4: Type MPO connector family - One fibre row
7. TIA-604-10, FOCIS 10B - Fiber Optic Connector Intermateability Standard- Type LC
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10. IEEE 802.3bs, 400 Gb/s Ethernet over optical fiber using multiple 25G/50G lane
11. SFF-8636, Management Interface for Cabled Environments (Rev 2.7)
12. SFF-8665, QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28) (Rev 1.9)
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14. QSFP-DD Hardware Specification for QSFP Double Density 8X Pluggable Transceiver, Rev 4.0 (Link QSFP-DD MSA)
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19. OIF2014.380.02, CEI-56G-LR-PAM4 Long Reach Interface (Apr 23, 2015)
20. SFF-8431, SFP+ 10Gb/s and Low-Speed Electrical Interface
21. SFF-8472, Diagnostic Monitoring Interface for Optical Transceivers
22. Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps and 25G+ bps I/O IA latest version
23. GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria
24. GR-63-CORE, NEBS Requirements
25. JESD8c.01, Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits
26. IEEE 802.3bm, 100G/40G Ethernet for optical fiber
27. CEI-56G-VSR-PAM4 Very Short Reach Interface, Latest Version
28. OIF-Thermal-01.0 – Implementation Agreement for Thermal Interface Specification for Pluggable Optics Modules (May 2015)

1. Introduction

1.1 Scope

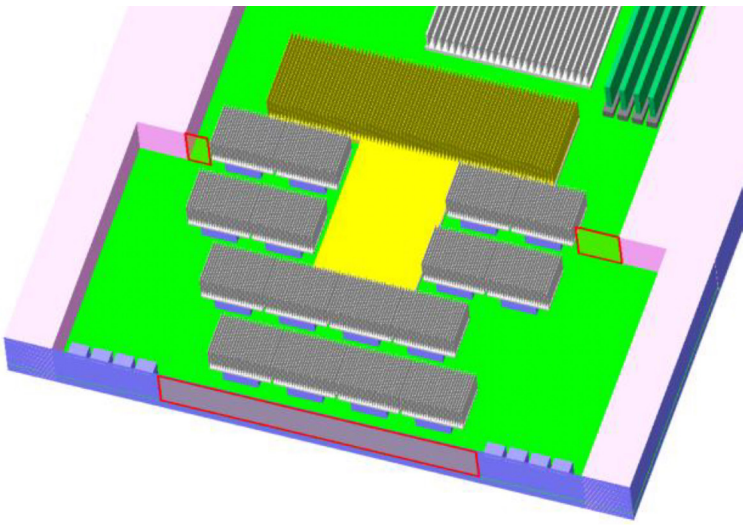
This specification defines the characteristics of an 8 and 16 lane On-Board Optics (OBOs) for use in up to 1× 400G and 2× 400G bandwidth capacity applications. and provides a common specification for systems manufacturers, system integrators, component manufacturers, and suppliers of on-board optics.

The specification defines electrical, mechanical, and thermal parameters for an On-Board Optic (OBO). It also includes normative requirements and informative guidance for the optical parameters.

The software management interface (memory map) is not in scope.

1.2 Data Center Reference Application

COBO has defined a primary reference application based on a shared generic design. The reference application is defined as an air cooled (with front to back airflow) 1RU modular 12.8T data center switch with one such depiction of a switch card shown in Figure 1-1. Variations on this reference application have been used to determine a number of COBO requirements.



1RU Modular 12.8T Switch Card with 16 OBOs, 2x400G each

Figure 1.1 - COBO Reference Application Example

1.3 OBO Configurations

This document considers high density 400G implementations in either a single 400G configuration or a high density 2x400G dual configuration as shown in Figure 1-2.

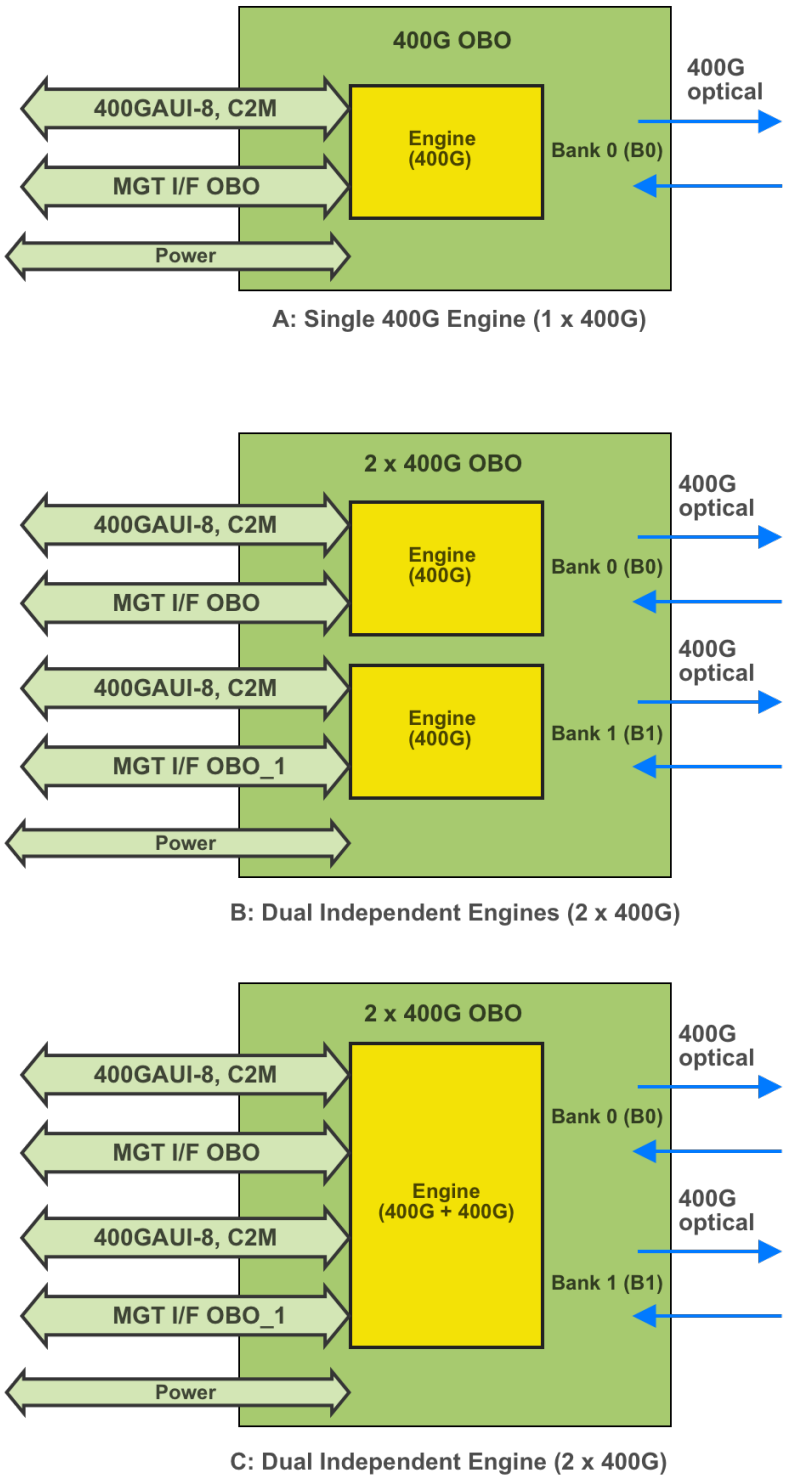


Figure 1.2 - OBO Configurations

Figure 1-2 shows three possible configurations of the 400G OBO. Figure 1-2A shows a single standalone 400G OBO. Figure 1-2B shows a dual 400G implementation where the internal architecture consists of two separate OBO optical engines. Figure 1-2C shows a dual 400G implementation where the internal architecture consists of two 400G optical engines integrated as a single OBO optical engine with two ports.

Figure 1-2B & C enable higher board density layouts by bundling 2 ports of 400G into a single OBO but appears to the host as two separable 400G OBOs.

1.4 High-Speed Electrical Configurations

The single OBO, eight-lane, supports eight high-speed data lanes (8 × 25GBd PAM4) and the dual OBO, sixteen-lane, supports two independent sets of eight high-speed data lanes (2 x 8 x 25GBd PAM4). The high-speed data interface for the OBO is based on 400GAUI-8 C2M. This document does not preclude usage of other baud rates up to the prescribed 25GBd.

1.5 Optical Configurations

This document does not define the optical physical layer; however, the OBO specification has been developed to be consistent with common industry standards for 400G front-panel pluggable modules.

The OBO may either be pigtailed or connectorized. Optical connectors should comply with industry conventions, see § 3.4.

1.6 Management Interface

The management interface uses the QSFP-DD Common MIS and communicates over a two-wire interface.

The dual OBO configurations shown in Figure 1-2 appear to the host as two separate single 400G optics for both the independent and integrated versions. Therefore, to support 16 optical lanes there are two separate memory maps supported by two independent two-wire interfaces.

2. Electrical Specifications

2.1 - Purpose and Applications

The electrical section specifies the different requirements for eight-lane and sixteen-lane COBO electrical channels which consist of a high-speed and low-speed connector. The electrical section includes the host PCB routing specifications, connector pinout and power supplies specifications. The drawing from Figure 2-1 provide a view of the OBO high-speed and low-speed connectors. The eight-lane and sixteen-lane high-speed connector supports up to eight and sixteen high-speed lanes respectively up to 25GBd. The eight-lane and sixteen-lane low-speed connector supports 28 and 56 contacts respectively for power and I/O's.

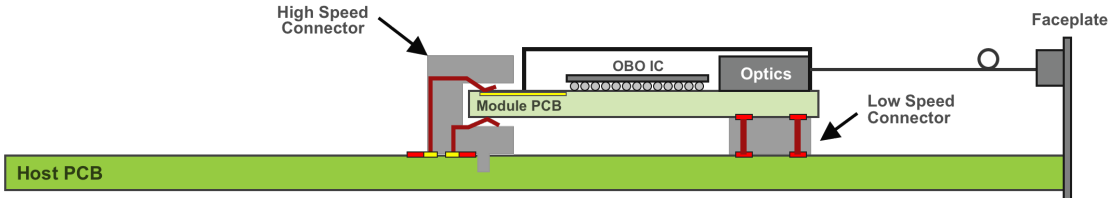


FIGURE 2.1 - Electrical Interface with Connectors - Side View

This section defines;

- High-speed and low-speed connector pinout and signal definitions
- Power supplies and return specifications

Figure 2-2 shows examples of block diagrams representing the different applications of OBOs.

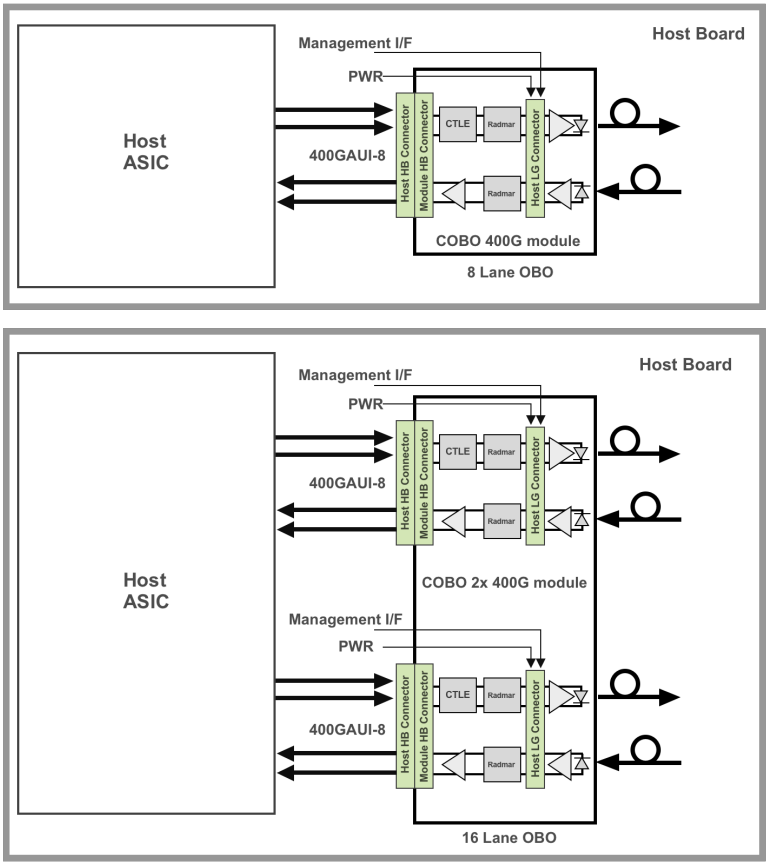


FIGURE 2.2 - COBO Applications Example

2.2 Clocking Considerations

2.2.1 Data Path Description

Within an OBO, host electrical and OBO media lanes are grouped together into a logical concept called a data path. A data path is intended to represent a group of lanes that will be powered up or down and initialized together. An example would include a 400GAUI-8 to 400GBASE-DR4 OBO implementation, where the data path would include eight host electrical lanes and four OBO media lanes.

2.2.2 Tx Clocking Considerations

Within a given Tx data path, the host is responsible for ensuring that all electrical lanes delivered to the OBO are frequency synchronous (sourced from the same clock domain). If an OBO supports multiple Tx data paths running concurrently, the different Tx data paths can either all be in a single clock domain or separate clock domains. The OBO advertises which of these two modes it supports via the management registers.

If the OBO supports multiple Tx data paths running concurrently in a single clock domain, the OBO shall ensure that active Tx data paths continue to operate undisturbed even as other Tx data paths (and their associated Tx input lanes) are enabled/disabled by the host.

2.2.3 Rx Clocking Considerations

Within a given Rx data path, all lanes received on the OBO media interface are required to be frequency synchronous (sourced from the same clock domain). If an OBO supports multiple Rx data paths running concurrently, the OBO shall allow the different Rx data paths to be asynchronous from each other (sourced from separate clock domains).

2.3 Electrical Connector – High-Speed

This section contains signal definitions and requirements that are specific to the OBO. The high-speed I/O's includes the connections between the host ASIC and OBO. The 400GAUI-8 C2M, interface support both 1 x 400G and 2 x 400G. For more information, see the appropriate electrical specifications for the electrical link, e.g., 802.3ba Annex 86A, 802.3bs Annex 120E or Annex 120C, FC-PI-6, FC-PI-7, OIF-CEI-28G-VSR, OIF-CEI-56G-VSR or the InfiniBand specification.

Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 2.3.1 and 2.3.2 may be used.

2.31 Rx(n) (p/n)

Rx(n)(p/n) are OBO receiver data outputs. Rx(n)(p/n) are AC-coupled 100Ω differential lines that should be terminated with 100Ω differentially at the Host ASIC. The AC coupling is inside the OBO and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to the limit in the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver data output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output as shown in §3.5.1;

- Rx1n/p to Rx8n/p is referred to Bank 0 for the eight-lane or sixteen-lane OBO.
- Rx1n/p_1 to Rx8n/p_1 is referred to Bank 1 for the sixteen-lane OBO

In the squelched state, output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp. In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the TWI. For specific details refer to CMIS latest version.

2.3.2 Tx(n)(p/n)

Tx(n)(p/n) are OBO transmitter data inputs. Tx (n)(p/n) are AC-coupled 100Ω differential lines with 100Ω differential terminations inside the OBO. The AC coupling is inside the OBO and not required on the Host board. The input signal complies with the relevant standard at the OBO input.

Output squelch, hereafter Tx Squelch, for loss of electrical signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, see § 3.5.1, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched;

- Tx1n/p to Tx8n/p is referred to Bank 0 for the eight-lane or sixteen-lane OBO.
- Tx1n/p_1 to Tx8n/p_1 is referred to Bank 1 for the sixteen-lane OBO.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In OBO operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the TWI. Tx Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided. For specific details refer to CMIS latest version.

2.3.3 Eight-Lane High-Speed Pins

The eight-lane high-speed edge connector consists of a single paddle card with 25 pads on the top and 25 pads on the bottom of the paddle card for a total of 50 pads.

See Figure 2-3 for the host top side pads signal symbols.

The pads are designed for a sequenced mating:

First mate – ground pads

Second mate - signal pads

See Figure 2-4 for the OBO pad numbering.

Refer to Table 2-1 for more pad description and Figure 4-15 for pad dimensions.

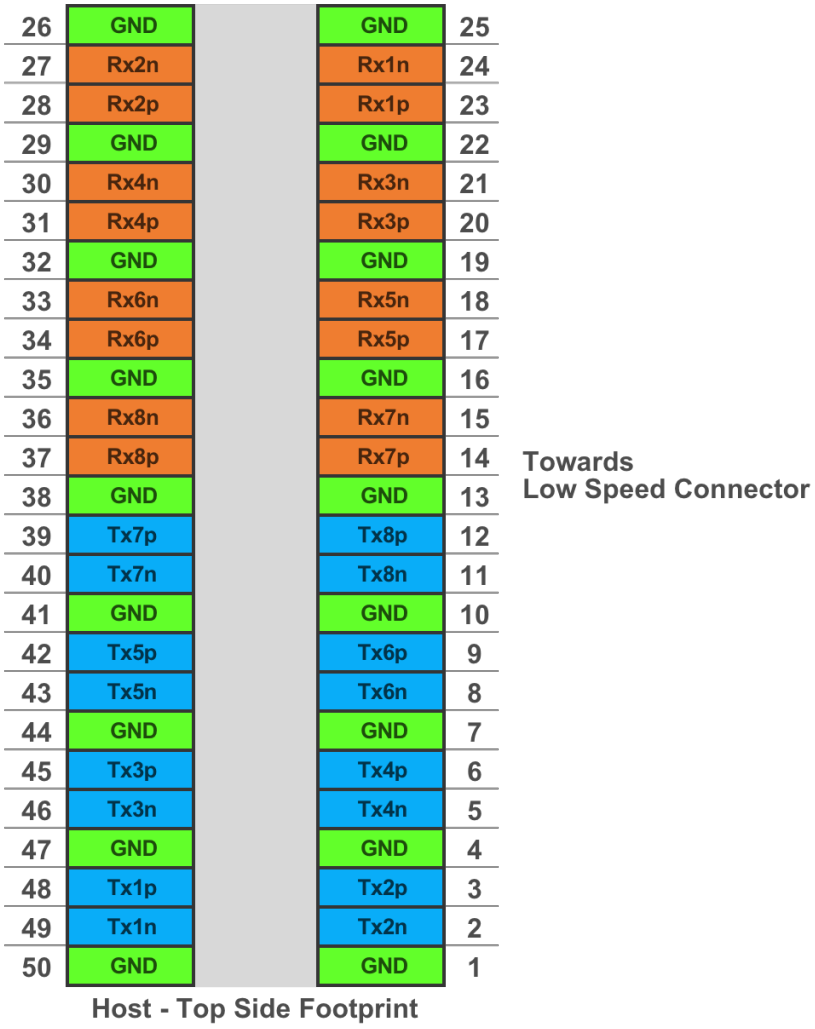


Figure 2-3: Host PCB High-Speed Connector Pads Eight-Lane - Top Side

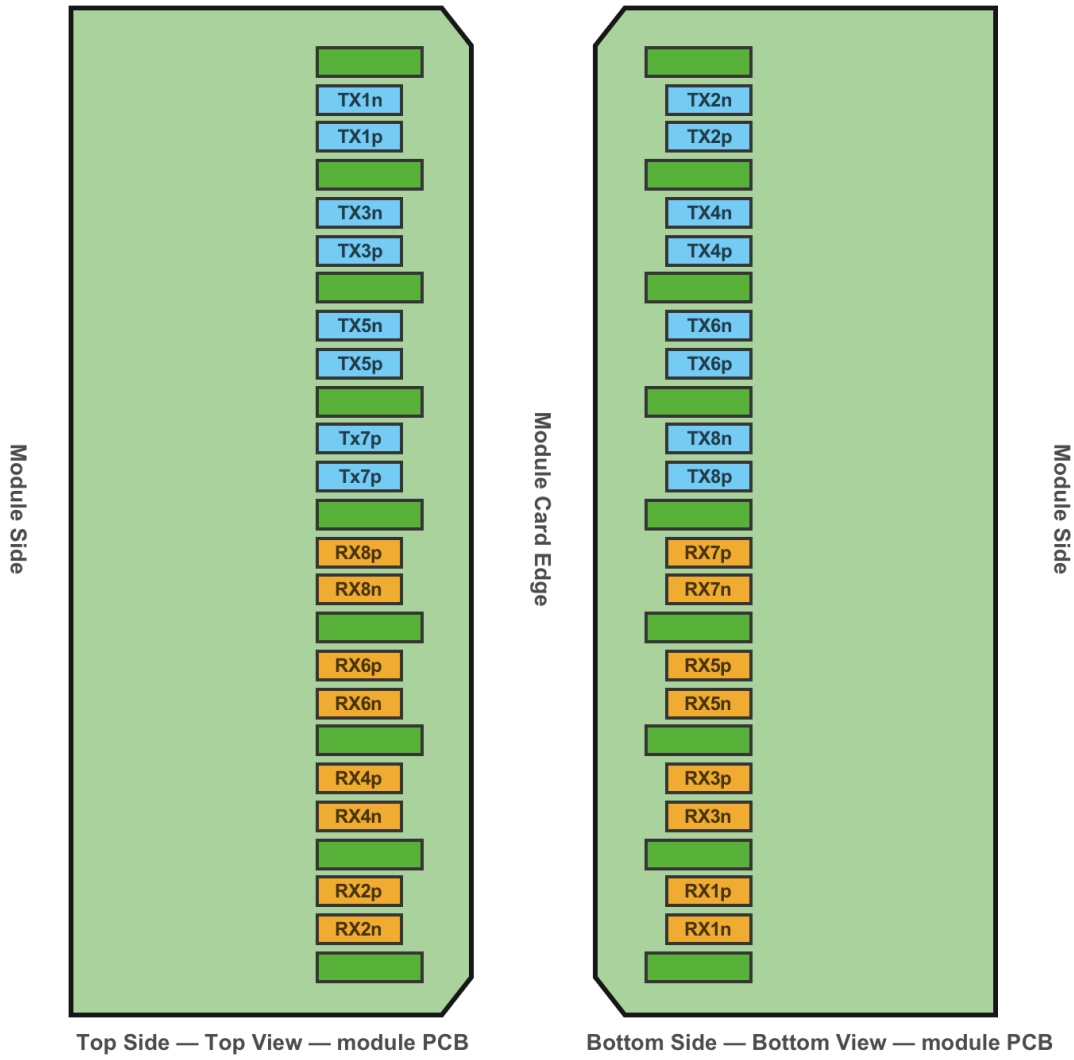


Figure 2-4: OBO PCB High-Speed Connector Pads - Eight-Lane

Host Pad	OBO Pad	Symbol	Description	Interface
1	1	GND	Ground	
2	2	Tx2N	Transmit Inverted Data Input	CML-I
3	3	Tx2P	Transmit Non-Inverted Data Input	CML-I
4	4	GND	Ground	
5	5	Tx4N	Transmit Inverted Data Input	CML-I
6	6	Tx4P	Transmit Non-Inverted Data Input	CML-I
7	7	GND	Ground	
8	8	Tx6N	Transmit Inverted Data Input	CML-I
9	9	Tx6P	Transmit Non-Inverted Data Input	CML-I
10	10	GND	Ground	
11	11	Tx8N	Transmit Inverted Data Input	CML-I
12	12	Tx8P	Transmit Non-Inverted Data Input	CML-I
13	13	GND	Ground	
14	14	Rx7P	Receive Non-Inverted Data Input	CML-O
15	15	Rx7N	Receive Inverted Data Input	CML-O
16	16	GND	Ground	
17	17	Rx5P	Receive Non-Inverted Data Input	CML-O
18	18	Rx5N	Receive Inverted Data Input	CML-O
19	19	GND	Ground	
20	20	Rx3P	Receive Non-Inverted Data Input	CML-O
21	21	Rx3N	Receive Inverted Data Input	CML-O
22	22	GND	Ground	
23	23	Rx1P	Receive Non-Inverted Data Input	CML-O
24	24	Rx1N	Receive Inverted Data Input	CML-O
25	25	GND	Ground	
26	26	GND	Ground	
27	27	Rx2N	Receive Inverted Data Input	CML-O
28	28	Rx2P	Receive Non-Inverted Data Input	CML-O
29	29	GND	Ground	
30	30	Rx4N	Receive Inverted Data Input	CML-O
31	31	Rx4P	Receive Non-Inverted Data Input	CML-O
32	32	GND	Ground	
33	33	Rx6N	Receive Inverted Data Input	CML-O
34	34	Rx6P	Receive Non-Inverted Data Input	CML-O
35	35	GND	Ground	
36	36	Rx8N	Receive Inverted Data Input	CML-O
37	37	Rx8P	Receive Non-Inverted Data Input	CML-O
38	38	GND	Ground	
39	39	Tx7P	Transmit Non-Inverted Data Input	CML-I
40	40	Tx7N	Transmit Inverted Data Input	CML-I
41	41	GND	Ground	
42	42	Tx5P	Transmit Non-Inverted Data Input	CML-I
43	43	Tx5N	Transmit Inverted Data Input	CML-I
44	44	GND	Ground	
45	45	Tx3P	Transmit Non-Inverted Data Input	CML-I
46	46	Tx3N	Transmit Inverted Data Input	CML-I
47	47	GND	Ground	
48	48	Tx1P	Transmit Non-Inverted Data Input	CML-I
49	49	Tx1N	Transmit Inverted Data Input	CML-I
50	50	GND	Ground	

Tabel 2-1: High-Speed Pins - Eight-Lane Pin Description

2.3.4 Sixteen-Lane High-Speed Pins

The sixteen-lane high-speed edge connector consists of a single paddle card with 50 pads on the top and 50 pads on the bottom of the paddle card for a total of 100 pads.

Figure 2-5 for the host top side pads signal symbols

The pads are designed for a sequenced mating:

First mate – ground pads

Second mate - signal pads

See Figure 2-6 for the OBO pad numbering.

Refer to Table 2-2 for more pad description and Figure 4-15 for pad dimensions.

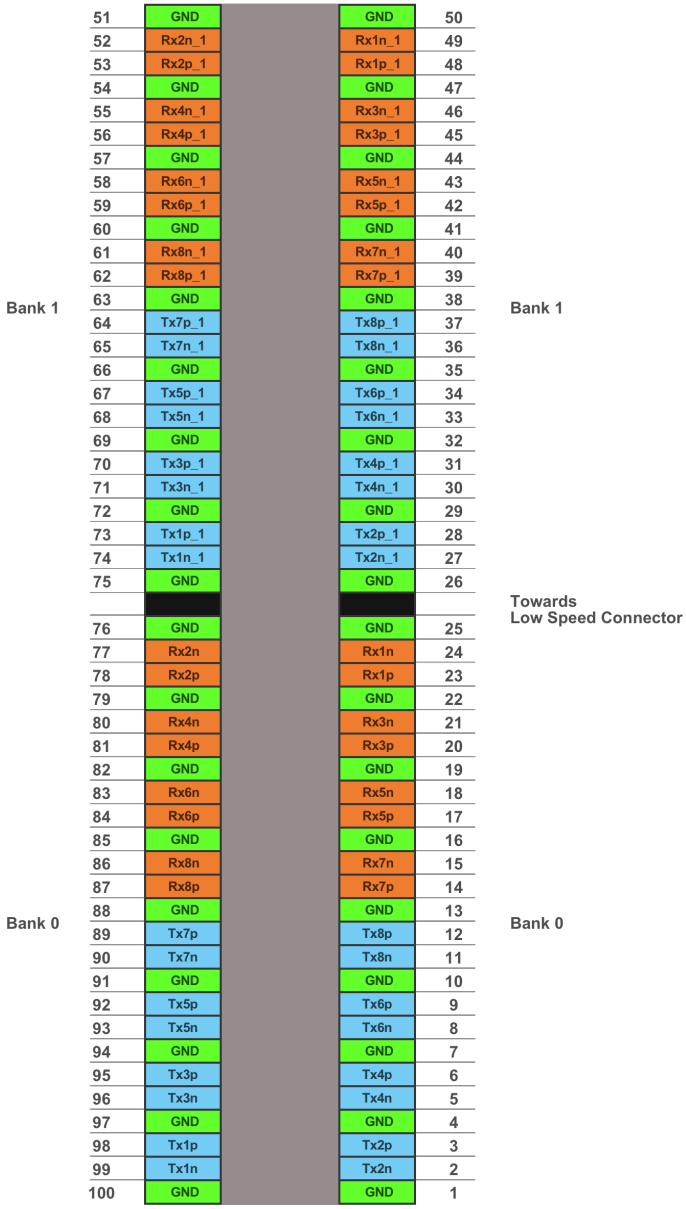


Figure 2-5: Host PCB High-Speed Connector Pads Sixteen-Lane - Top Side

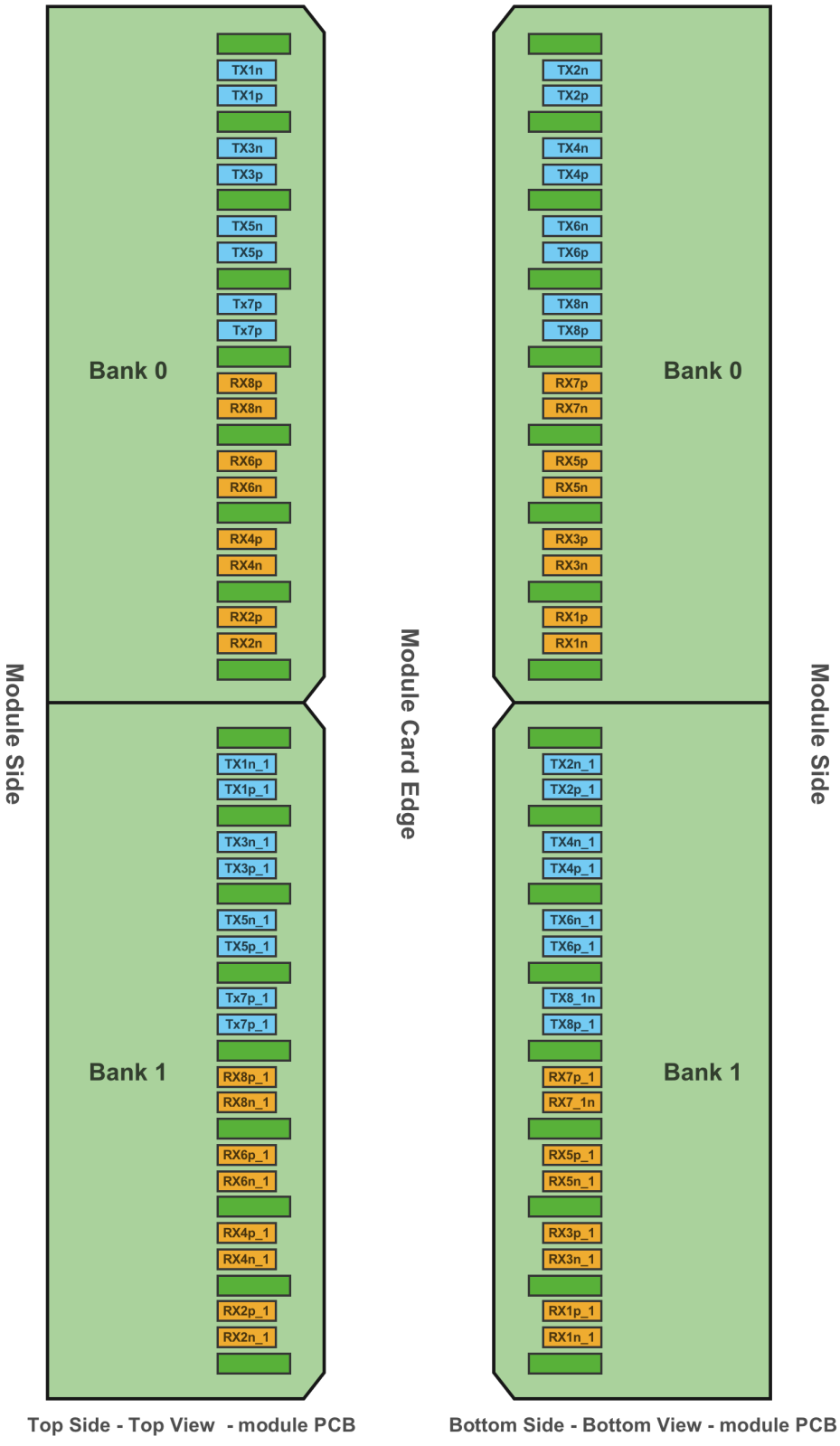


Figure 2-6: OBO PCB High-speed Connector Pads - Sixteen-Lane

Host Pad	OBO Pad	Symbol	Description	Bank	Interface
1	1	GND	Ground	0	
2	2	Tx2n	Transmit Inverted Data Input	0	CML-I
3	3	Tx2p	Transmit Non-Inverted Data Input	0	CML-I
4	4	GND	Ground	0	
5	5	Tx4n	Transmit Inverted Data Input	0	CML-I
6	6	Tx4p	Transmit Non-Inverted Data Input	0	CML-I
7	7	GND	Ground	0	
8	8	Tx6n	Transmit Inverted Data Input	0	CML-I
9	9	Tx6p	Transmit Non-Inverted Data Input	0	CML-I
10	10	GND	Ground	0	
11	11	Tx8n	Transmit Inverted Data Input	0	CML-I
12	12	Tx8p	Transmit Non-Inverted Data Input	0	CML-I
13	13	GND	Ground	0	
14	14	Rx7p	Receive Non-Inverted Data Input	0	CML-O
15	15	Rx7n	Receive Inverted Data Input	0	CML-O
16	16	GND	Ground	0	
17	17	Rx5p	Receive Non-Inverted Data Input	0	CML-O
18	18	Rx5n	Receive Inverted Data Input	0	CML-O
19	19	GND	Ground	0	
20	20	Rx3p	Receive Non-Inverted Data Input	0	CML-O
21	21	Rx3n	Receive Inverted Data Input	0	CML-O
22	22	GND	Ground	0	
23	23	Rx1p	Receive Non-Inverted Data Input	0	CML-O
24	24	Rx1n	Receive Inverted Data Input	0	CML-O
25	25	GND	Ground	0	
26	26	GND	Ground	1	
27	27	Tx2n_1	Transmit Inverted Data Input	1	CML-I
28	28	Tx2p_1	Transmit Non-Inverted Data Input	1	CML-I
29	29	GND	Ground	1	
30	30	Tx4n_1	Transmit Inverted Data Input	1	CML-I
31	31	Tx4p_1	Transmit Non-Inverted Data Input	1	CML-I
32	32	GND	Ground	1	
33	33	Tx6n_1	Transmit Inverted Data Input	1	CML-I
34	34	Tx6p_1	Transmit Non-Inverted Data Input	1	CML-I
35	35	GND	Ground	1	
36	36	Tx8n_1	Transmit Inverted Data Input	1	CML-I
37	37	Tx8p_1	Transmit Non-Inverted Data Input	1	CML-I
38	38	GND	Ground	1	
39	39	Rx7p_1	Receive Non-Inverted Data Input	1	CML-O
40	40	Rx7n_1	Receive Inverted Data Input	1	CML-O
41	41	GND	Ground	1	
42	42	Rx5p_1	Receive Non-Inverted Data Input	1	CML-O
43	43	Rx5n_1	Receive Inverted Data Input	1	CML-O
44	44	GND	Ground	1	
45	45	Rx3p_1	Receive Non-Inverted Data Input	1	CML-O
46	46	Rx3n_1	Receive Inverted Data Input	1	CML-O
47	47	GND	Ground	1	
48	48	Rx1p_1	Receive Non-Inverted Data Input	1	CML-O
49	49	Rx1n_1	Receive Inverted Data Input	1	CML-O
50	50	GND	Ground	1	
51	51	GND	Ground	1	
52	52	Rx2n_1	Receive Inverted Data Input	1	CML-O
53	53	Rx2p_1	Receive Non-Inverted Data Input	1	CML-O
54	54	GND	Ground	1	
55	55	Rx4n_1	Receive Inverted Data Input	1	CML-O
56	56	Rx4p_1	Receive Non-Inverted Data Input	1	CML-O

Table 2-2: –High-Speed I/O Pins OBO - Sixteen Lane Pin Description

57	57	GND	Ground	I	
58	58	Rx6n_I	Receive Inverted Data Input	I	CML-O
59	59	Rx6p_I	Receive Non-Inverted Data Input	I	CML-O
60	60	GND	Ground	I	
61	61	Rx8n_I	Receive Inverted Data Input	I	CML-O
62	62	Rx8p_I	Receive Non-Inverted Data Input	I	CML-O
63	63	GND	Ground	I	
64	64	Tx7p_I	Transmit Non-Inverted Data Input	I	CML-I
65	65	Tx7n_I	Transmit Inverted Data Input	I	CML-I
66	66	GND	Ground	I	
67	67	Tx5p_I	Transmit Non-Inverted Data Input	I	CML-I
68	68	Tx5n_I	Transmit Inverted Data Input	I	CML-I
69	69	GND	Ground	I	
70	70	Tx3p_I	Transmit Non-Inverted Data Input	I	CML-I
71	71	Tx3n_I	Transmit Inverted Data Input	I	CML-I
72	72	GND	Ground	I	
73	73	Tx1p_I	Transmit Non-Inverted Data Input	I	CML-I
74	74	Tx1n_I	Transmit Inverted Data Input	I	CML-I
75	75	GND	Ground	I	
76	76	GND	Ground	0	
77	77	Rx2n	Receive Inverted Data Input	0	CML-O
78	78	Rx2p	Receive Non-Inverted Data Input	0	CML-O
79	79	GND	Ground	0	
80	80	Rx4n	Receive Inverted Data Input	0	CML-O
81	81	Rx4p	Receive Non-Inverted Data Input	0	CML-O
82	82	GND	Ground	0	
83	83	Rx6n	Receive Inverted Data Input	0	CML-O
84	84	Rx6p	Receive Non-Inverted Data Input	0	CML-O
85	85	GND	Ground	0	
86	86	Rx8n	Receive Inverted Data Input	0	CML-O
87	87	Rx8p	Receive Non-Inverted Data Input	0	CML-O
88	88	GND	Ground	0	
89	89	Tx7p	Transmit Non-Inverted Data Input	0	CML-I
90	90	Tx7n	Transmit Inverted Data Input	0	CML-I
91	91	GND	Ground	0	
92	92	Tx5p	Transmit Non-Inverted Data Input	0	CML-I
93	93	Tx5n	Transmit Inverted Data Input	0	CML-I
94	94	GND	Ground	0	
95	95	Tx3p	Transmit Non-Inverted Data Input	0	CML-I
96	96	Tx3n	Transmit Inverted Data Input	0	CML-I
97	97	GND	Ground	0	
98	98	Tx1p	Transmit Non-Inverted Data Input	0	CML-I
99	99	Tx1n	Transmit Inverted Data Input	0	CML-I
100	100	GND	Ground	0	

Table 2-2: –High-Speed I/O Pins OBO - Sixteen Lane Pin Description (con't)

2.4 Electrical Connector – Low-Speed

The low-speed connector for the eight-lane and sixteen lane OBO has the following low-speed pins for control, power and status to support the different OBO applications. The definitions are for eight-lane and sixteen-lane low-speed definitions.

- Bank 0 of the sixteen-lane uses the same definitions as the eight-lane.
- Bank 1 of the sixteen-lane uses the suffix "_1".

2.4.1.1 RxLOS

The RxLOS signal is intended as an indication to the host in which the OBO is installed that the primary port optical input signal strength is below a certain threshold.

RxLOS may be an optional function depending on the supported standard. If the RxLOS function is not implemented, or is reported via the two-wire interface only, the RxLOS contact shall be held low using a pull down of 1kΩ by the OBO. This pin can be useful for SyncE applications.

The RxLOS is an open drain/collector output from the OBO and for a nominally 3.3V VCC, the resistive pull up to VCC on the Host shall be in the range 4.7kΩ to 10kΩ.

Rx_LOS assert min (ton_rxdis) and de-assert max (toff_rxdis) are defined in the relevant standard.
Sixteen-lane uses RXLOS and RXLOS_1.

2.4.1.2 ResetL

ResetL is an input control to the OBO. A low level on the ResetL pin longer than the minimum pulse length (t_RESET_init) initiates an OBO module reset and all user OBO settings to their default state.

The ResetL shall be pulled up to VCC in the OBO. Sixteen-lane uses ResetL and ResetL_1.

2.4.1.3 ModSelL

The ModSelL is an input signal. When held low by the host, the OBO communication interface is active on the single TWI bus. When ModSelL is "High", the OBO shall not respond to or acknowledge any TWI communication from the host.

In order to avoid conflicts, the host system shall not attempt TWI communications within the ModSelL de-assert time after any OBO modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected OBO. The assertion and de-asserting periods of different OBOs may overlap as long as the above timing requirements are met.

The ModSelL shall be pulled up to VCC in the OBO. Sixteen-lane uses ModSelL and ModselL_1.

2.4.1.4 IntL

Interrupt request from OBO to host is an output signal. When the IntL is asserted low, it indicates a change in the OBO state, a possible OBO operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI or other communication channel. The IntL signal is deasserted High after all set interrupt flags are read.

The signal is an open collector output and must be pulled up to VCC Host on the host board.

Sixteen lane uses IntL and IntL_1.

2.4.1.5 OUTp/OUTn or RxMCLKp/RxMCLKn

The signals are CML outputs. Example illustrative function could either be used for a low frequency output differential clock; RxMCLKp/n, in phase with the primary optical port Rx data. This can be useful for SyncE applications. Or another illustrative example could be a faster communication channel, OUTp/n, support.

Sixteen-lane uses:

OUTp/OUTn or RxMCLKp/RxMCLKn and OUTp_1/OUTn_1 or RxMCLKp_1/RxMCLKn_1.

2.4.1.6 INp/INn

INp and INn are differential CML inputs. Example illustrative function could be a faster communication channel support.

The inputs shall be AC coupled inside the OBO.

Sixteen-lane uses INp/INn and INp_1/INn_1.

2.4.1.7 MosPrsL

ModPrsL must be pulled up to VCC Host on the host board and pulled low in the OBO. The ModPrsL is asserted "Low" by the OBO when the OBO is inserted.

ModPrsL must be pulled up to VCC Host with a resistor in the range of 4.7k to 10k on the host board and pulled low in the OBO.

Sixteen-lane uses one ModPrsL.

2.4.1.8 Tx_Disable

When Tx_Disable is asserted high or left open, the OBO's transmitter output shall be turned off. When the TX_Disable is asserted low, the OBO's transmitter is operating normally.

TX_Disable signal shall be pulled up to VCC in the OBO.

Sixteen-lane uses Tx_Disable and Tx_Disable_1.

2.4.1.9 RxLOSAlt

The RXLOSAlt output signal is intended as an indication to the host in which the OBO is installed that a secondary port optical input signal strength is below a certain threshold. This can be useful for SyncE applications.

The RxLOSAlt is an open drain/collector output from the OBO.

For a nominally 3.3V VCC, the resistive pull up to VCC on the Host shall be in the range 4.7k to 10k.

Sixteen-lane uses RxLOSAlt and RxLOSAlt_1.

2.4.1.10 InitMODE

The InitMode signal allows the host to define whether the OBO will initialize under host software control (InitMode asserted High) or hardware control (InitMode deasserted Low).

The InitMode input signal shall be pulled up to VCC inside the OBO.

See “CMIS xx-xx” for more information.

Sixteen-lane uses InitMODE and InitMODE_1.

2.4.1.11 SCL

2-wire serial clock signal. Requires pull-up to 3.3V on host.

Sixteen-lane uses SCL and SCL_1.

Refer to § 2.6 for further details.

2.4.1.12 SDA

2-wire serial data signal. Requires pull-up to 3.3V on host.

Sixteen-lane uses SDA and SDA_1.

Refer to § 2.6 for further details.

2.4.1.13 REFCLKp/REFCLKn

The REFCLKp and REFCLKn are CML input clocks. The purpose of the input reference clock is to act as a low jitter transmit reference.

Sixteen-lane uses REFCLKp/REFCLKn and REFCLKp_1/REFCLKn_1.

For application requiring different transmitter clock sources, egress direction, the OBO shall report clock recovery capabilities.

See latest CMIS “TX input clock recover capabilities” for further details.

2.4.1.14 VCC

3.3V nominal supply.

Each low-speed connector pins provides up to 1.5 amps for a total of 6 amps (19.8 watts nominal).

Refer to § 2.4.

2.4.1.15 Return (GND)

OBO Ground. Logic and power return path.

2.4.2 Eight and Sixteen Low-Speed Pin Locations

The OBO eight-lane low-speed connector consists of 28 pads on the bottom. The pads are defined in such a manner to accommodate insertion of an OBO into an OBO receptacle.

Refer to Figure 2-7 and Table 2-3 for more information.

The OBO sixteen-lane low-speed connector consists of 56 pads on the bottom. The pads are defined in such a manner to accommodate insertion of an OBO into an OBO receptacle.

Refer to Figure 2-8 and Table 2-4 for more information.

The pads are designed for a sequenced mating:

- First mate – ground pads

  Eight Lane: Extended between A3-B3 and A12-B12. See Figure 2-7

  Sixteen Lane: Extended between A3-B3, A12-B12, A17-B17 and A26-B26. See Figure 2-8.
- Second mate – VCC pads
- Third mate – signal pads

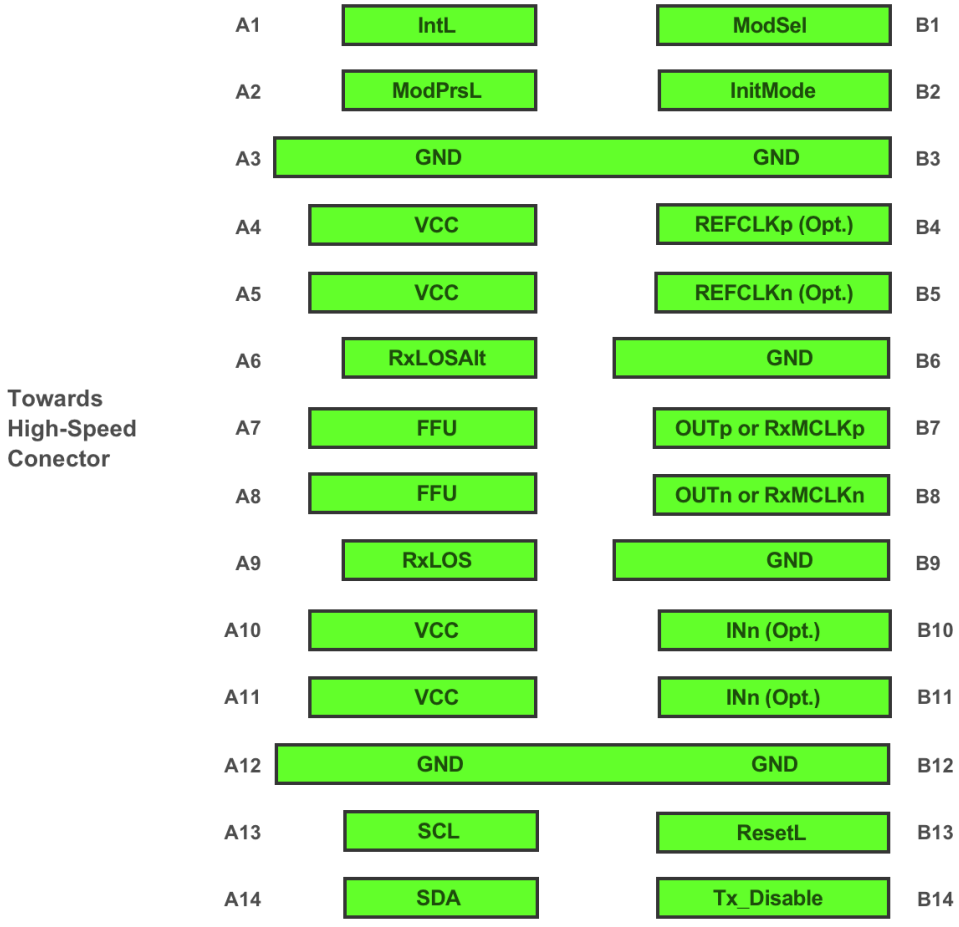


Table 2-7: Eight Lane OBO Low-Speed Pins – Paddle Card Bottom Pads

Host Pad	OBO Pad	Symbol	Description	Bank	Interface
A1	A1	IntL	Interrupt	0	LVTTL-O
A2	A2	ModPrsL	OBO Presence	0	LVTTL-O
A3	A3	GND	Return	0	
A4	A4	VCC	+3.3V Power Supply	0	
A5	A5	VCC	+3.3V Power Supply	0	
A6	A6	RxLOSAlt	Receiver Loss of Signal Alternate	0	LVTTL-O
A7	A7	FFU	For Future Use	0	
A8	A8	FFU	For Future Use	0	
A9	A9	RxLOS	Receiver Loss of Signal	0	LVTTL-O
A10	A10	VCC	+3.3V Power Supply	0	
A11	A11	VCC	+3.3V Power Supply	0	
A12	A12	GND	Return	0	
A13	A13	SCL	Two-wire serial interface clock	0	LVCMOS I/O
A14	A14	SDA	Two-wire serial interface data	0	LVCMOS I/O
B1	B1	ModSel	OBO Select	0	LVTTL-I
B2	B2	InitMode	Initialization Mode	0	LVTTL-I
B3	B3	GND	Return	0	
B4	B4	REFCLKp (opt)	Reference Clock p – Optional	0	CML-I
B5	B5	REFCLKn (opt)	Reference Clock n – Optional	0	CML-I
B6	B6	GND	Return	0	
B7	B7	OUTp or RxMCLKp	Communication Output p or Clock Monitor p– Optional	0	CML-O
B8	B8	OUTn or RxMCLKn	Communication Output n or Clock Monitor n – Optional	0	CML-O
B9	B9	GND	Return	0	
B10	B10	INp (opt)	Communication Input p – Optional	0	CML-I
B11	B11	Inn (opt)	Communication Input n – Optional	0	CML-I
B12	B12	GND	Return	0	
B13	B13	ResetL	OBO RESET	0	LVTTL-I
B14	B14	Tx_Disable	Transmit Disable	0	LVTTL-I

Table 2.3: Eight Lane Low-Speed Pins

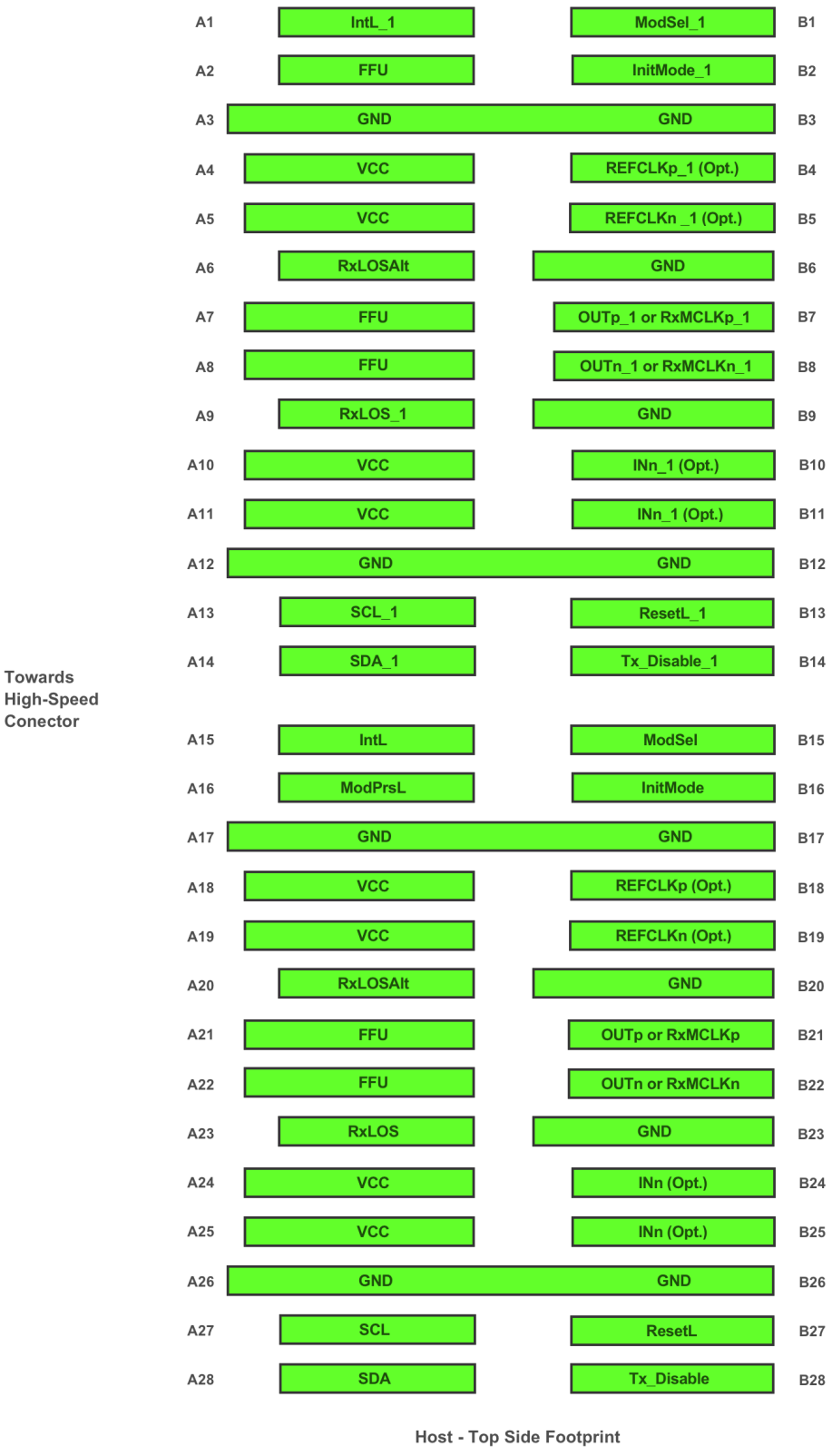


Table 2-8: Sixteen Lane OBO Low-Speed Pins – Paddle Card Bottom Pads

Host Pad	OBO Pad	Symbol	Description	Bank	Interface
A1	A1	IntL_I	Interrupt	I	LVTTL-O
A2	A2	FFU	For Future Use	I	LVTTL-O
A3	A3	GND	Return	I	
A4	A4	VCC	+3.3V Power Supply	I	
A5	A5	VCC	+3.3V Power Supply	I	
A6	A6	RxLOSAlt_I	Receiver Loss of Signal Alternate	I	LVTTL-O
A7	A7	FFU	For Future Use	I	
A8	A8	FFU	For Future Use	I	
A9	A9	RxLOS_I	Receiver Loss of Signal	I	LVTTL-O
A10	A10	VCC	+3.3V Power Supply	I	
A11	A11	VCC	+3.3V Power Supply	I	
A12	A12	GND	Return	I	
A13	A13	SCL_I	Two-wire serial interface clock	I	LVCMOS I/O
A14	A14	SDA_I	Two-wire serial interface data	I	LVCMOS I/O
A15	A15	IntL	Interrupt	0	LVTTL-O
A16	A16	ModPrsL	OBO Presence	0	LVTTL-O
A17	A17	GND	Return	0	
A18	A18	VCC	+3.3V Power Supply	0	
A19	A19	VCC	+3.3V Power Supply	0	
A20	A20	RxLOSAlt	Receiver Loss of Signal Alternate	0	LVTTL-O
A21	A21	FFU	For Future Use	0	
A22	A22	FFU	For Future Use	0	
A23	A23	RxLOS	Receiver Loss of Signal	0	LVTTL-O
A24	A24	VCC	+3.3V Power Supply	0	
A25	A25	VCC	+3.3V Power Supply	0	
A26	A26	GND	Return	0	
A27	A27	SCL	Two-wire serial interface clock	0	LVCMOS I/O
A28	A28	SDA	Two-wire serial interface data	0	LVCMOS I/O
B1	B1	ModSel_I	OBO Select	I	LVTTL-I
B2	B2	InitMode_I	Initialization Mode	I	LVTTL-I
B3	B3	GND	Return	I	
B4	B4	REFCLKp_I (opt)	Reference Clock p – Optional	I	CML-I
B5	B5	REFCLKn_I (opt)	Reference Clock n – Optional	I	CML-I
B6	B6	GND	Return	I	
B7	B7	OUTp_I or RxMCLKp_I	Communication Output p or Clock Monitor p– Optional	I	CML-O
B8	B8	OUTn_I or RxMCLKn_I	Communication Output n or Clock Monitor n – Optional	I	CML-O
B9	B9	GND	Return	I	
B10	B10	INp_I (opt)	Communication Input p – Optional	I	CML-I
B11	B11	INp_I (opt)	Communication Input n – Optional	I	CML-I
B12	B12	GND	Return	I	
B13	B13	ResetL_I	OBO RESET	I	LVTTL-I
B14	B14	Tx_Disable_I	Transmit Disable	I	LVTTL-I
B15	B15	ModSel	OBO Select	0	LVTTL-I
B16	B16	InitMode	Initialization Mode	0	LVTTL-I
B17	B17	GND	Return	0	
B18	B18	REFCLKp (opt)	Reference Clock p – Optional	0	CML-I
B19	B19	REFCLKn (opt)	Reference Clock n – Optional	0	CML-I
B20	B20	GND	Return	0	
B21	B21	OUTp or RxMCLKp	Communication Output p or Clock Monitor p– Optional	0	CML-O
B22	B22	OUTn or RxMCLKn	Communication Output n or Clock Monitor n – Optional	0	CML-O
B23	B23	GND	Return	0	
B24	B24	INp (opt)	Communication Input p – Optional	0	CML-I
B25	B25	Inn (opt)	Communication Input n – Optional	0	CML-I
B26	B26	GND	Return	0	
B27	B27	ResetL	OBO RESET	0	LVTTL-I
B28	B28	Tx_Disable	Transmit Disable	0	LVTTL-I

Table 2.4: Sixteen Lane Low-Speed Pins

2.4.3 Application Schematic

Figure 2-9, Figure 2-10, Figure 2-11 and Figure 2-12 show examples of OBO host PCB schematics with connections to CDR and control ICs. An eight wide and sixteen wide electrical/optical interface is shown. Note that other configurations are supported including implementations employing optical multiplexing (WDM) or electrical multiplexing.

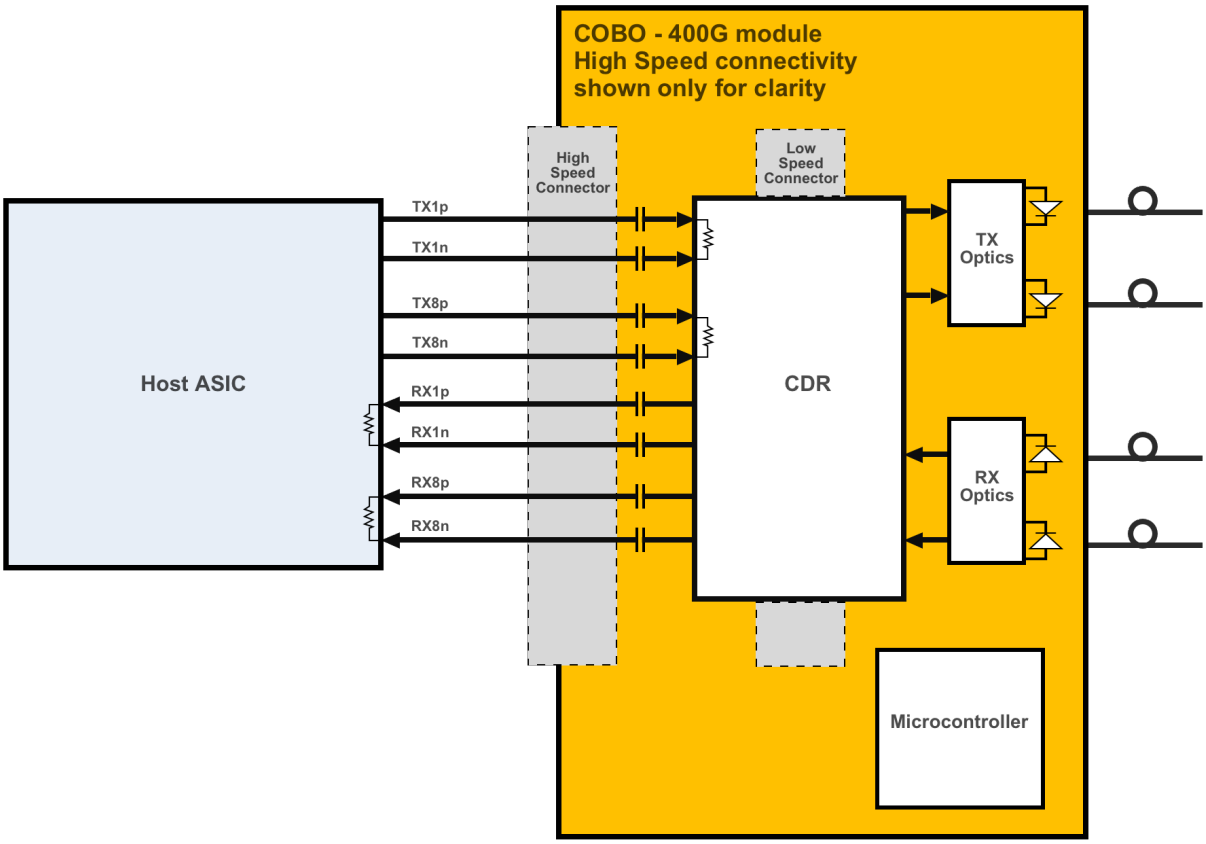


Figure 2.9: Eight Lane Host High-Speed Schematic Example

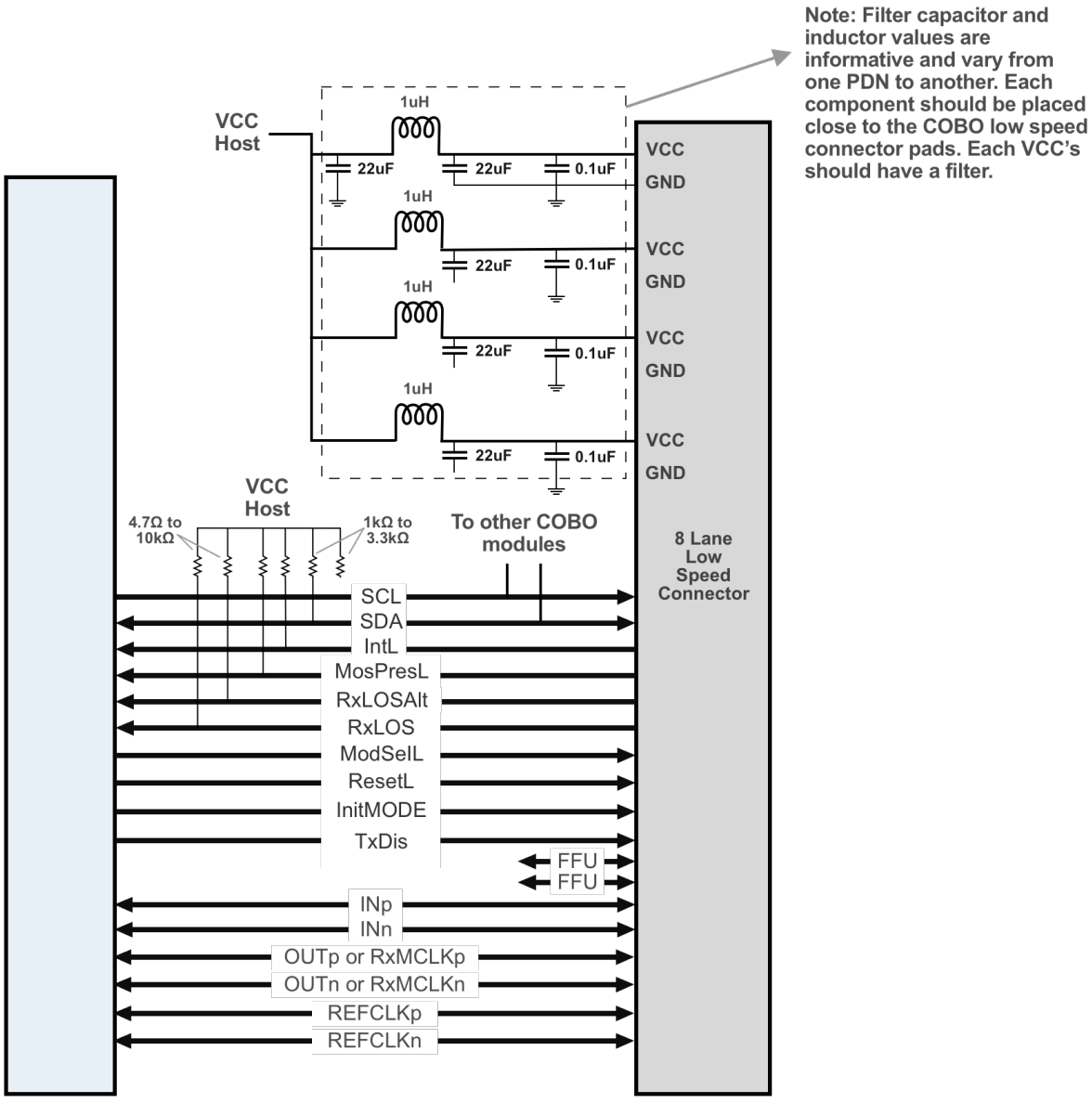


Figure 2-10: Eight-Lane Host Low-Speed Schematic Example

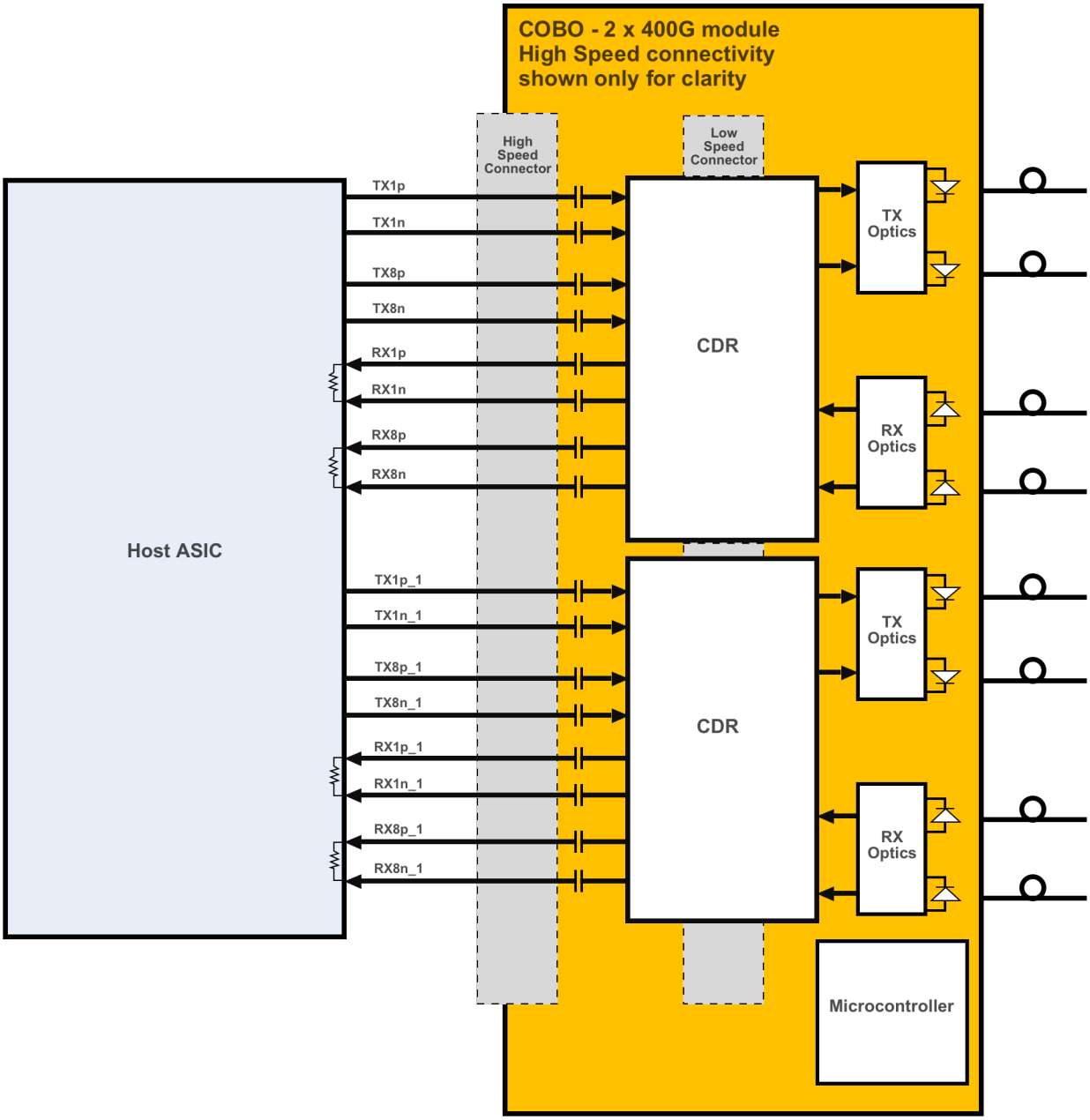


Figure 2-11: Sixteen-Lane Host High-Speed Schematic Example

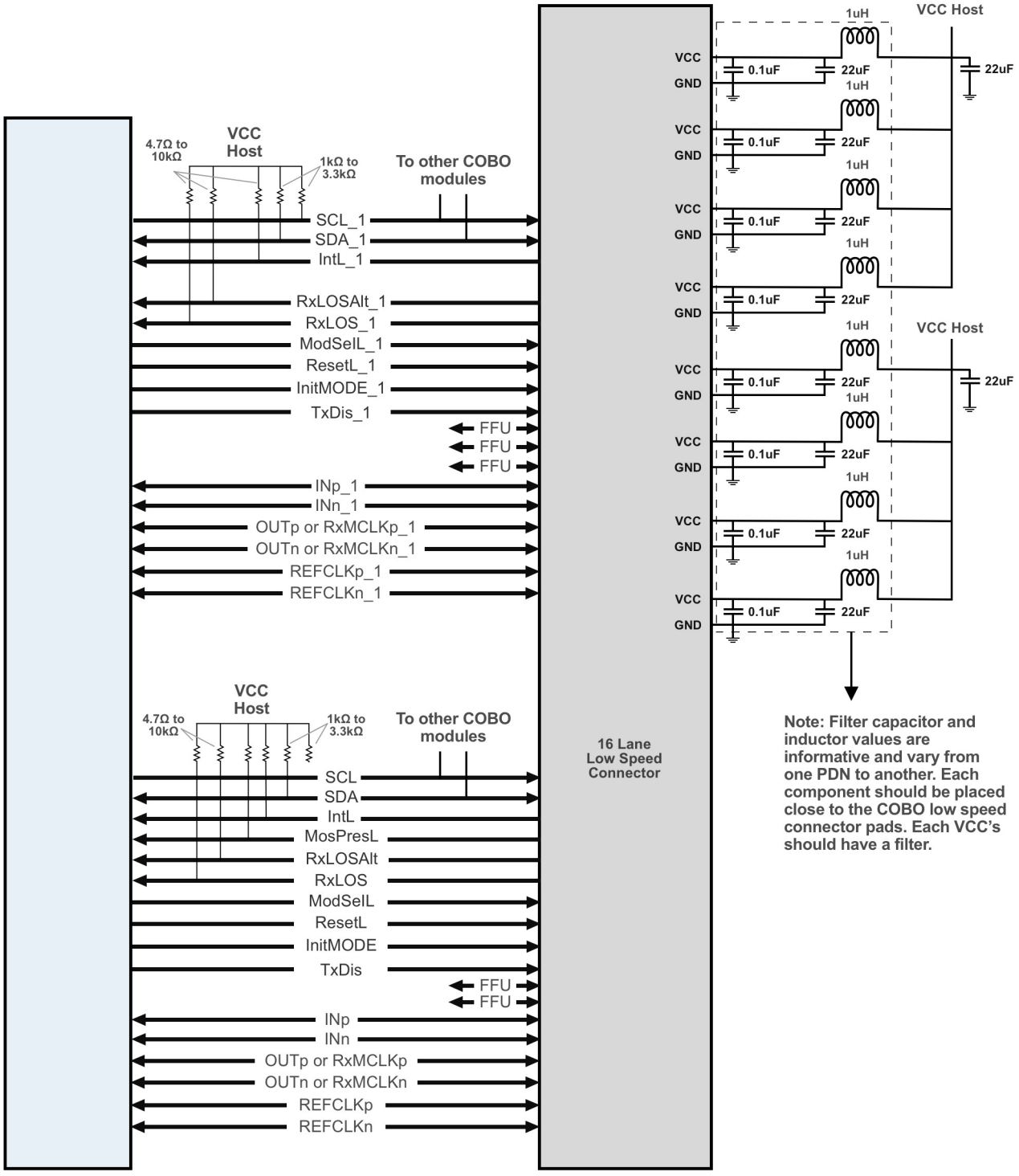


Figure 2-12: Sixteen-Lane Host Low-Speed Schematic Example

2.4.4 Low-Speed Electrical Specifications

The low-speed signaling other than the SCL, SDA and the differential optional interface is based on Low Voltage TTL (LVTTL) operating at VCC. Hosts shall use a pull-up resistor connected to VCC host on each of the TWI SCL (clock), SDA (data), and all low-speed status outputs in Table 2-5.

Note: Timing diagrams for SCL and SDA are shown in § 2.6.

Parameters	Symbol	Min	Max	Unit	Note
SDA and SCL Output	VOL	0	0.4	V	IOL (max.) = 3 mA for standard-mode and Fast-mode, or 20 mA for Fast-mode Plus
	VOH	Vcc-0.5	VCC+0.3	V	
SCA and SCL Input	VIL	-0.3	VCC*0.3	V	Input ref set to 30% of VDD
	VIH	VCC*0.7	VCC+0.5	V	Input ref set to 70% of VDD
Capacitance for SDA and SCL signal	Ci		14	pF	
Total bus capacitance load (SDA and SCL)	Cb		100	pF	For 400kHz clock rate use 3.0 k Ohms Pullup resistor, max.
			200	pF	For 400kHz clock rate use 1.6 k Ohms pullup resistor, max.
RxLos and RxLosAlt	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	4.7kΩ to 10Ω Pull up to Host VCC
InitMode,Reseth, ModSel,Tx_Disable	VIL	-0.3	0.8	V	
	VIH	2.0	VCC+0.3	V	
	I Iin I		360	uA	OV<Vin<VCC
IntL	VOL	0	0.4	V	IOL = 2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10Ω Pull up to Host VCC
ModPrsL	VOL	0	0.4	V	IOL = 2.0mA
	VOH	VCC-0.5	VCC+0.3	V	4.7k to 10k Pull up to Host VCC
INp / INn (optional)	Freq.		3.0	GHz	Differential CML-I 100-ohm nominal - AC coupled in OBO
OUTp/OUTn or RxMCLKp/RxMCLKn (optional)	Freq.		3.0	GHz	Differential CML-I 100-ohm nominal - AC coupled in OBO
REFCLKp/REFCLKn (optional)	Freq.		3.0	GHz	Differential CML-I 100-ohm nominal - AC coupled in OBO

Table 2-5: Low-Speed OBO Electrical Specifications

2.4.5 Timing for Soft Control and Status Functions

Parameters	Symbol	Max	Unit	Conditions
Initialization Time	MgmtInitDuration	2000	ms	Time from power on[1] or rising edge of Reset until the OBO is fully functional.
ResetL Assert Time	t_RESET_init	10	us	Minimum pulse time on the ResetL signal to initiate an OBO reset.
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout: IntL=Vol
IntL Deassert Time	toff_IntL	500	us	Time from clear on read2 operation of associated flag until Vout: IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = lb) and IntL asserted
Rx LOS Assert Time (optional fast mode)	ton_losf	1	ms	Time from Rx LOS state to Rx LOS bit set (value = lb) and IntL asserted.
Rx LOS Deassert Time (optional fast mode)	toff_losf	3	ms	Time from Rx LOS condition absents to negation of Rx LOS status bit.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value =lb)2 until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = Ob)2 until Rx output rises above 90% of nominal
Tx Fault Assert Time	ton_Txfault	200	m	Time from Tx Fault state to Tx Fault bit set (value=lb) and IntL asserted.
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=lb) and IntL asserted.
Mask Assert Time	ton_mask	100	ms	Time from mask bit set (value=lb)3 until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value=0b)3 until associated IntL operation resumes
Module Select Wait Time DataPathDeinit Max Duration DataPathInit Max Duration ModulePwrDn Max Duration	ModSelL Wait Time DataPathDeinit_MaxDuration DataPathInit_MaxDuration ModulePwrDn_MaxDuration	--	--	See CMIS "Table 40- Implemented Management Interface Features Advertising"

Table 2-6: Timing For OBO Soft Control Functions

Note 1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 2-8.

Note 2. Measured from the rising edge of SDA in the stop bit of the read transaction.

Note 3. Measured from the rising edge of SDA in the stop bit of the write transaction.

Note 4. Rx LOS condition is defined at the optical input by the relevant standard.

2.4.6 Squelch and Disable Timing

Squelch and disable timing are defined in Table 2-7 below.

Parameters	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached. See subsection 2.3.1
Rx Squelch Deassert Time	toff_Rxsq	15	ms	Time from resumption of Rx input signal until normal Rx output condition is reached. See subsection 2.3.1
Rx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until normal Tx output condition is reached. See subsection 2.3.2
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See subsection 2.3.2
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence[1] until optical output falls below 10% of nominal
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)1 until optical output falls below 10% of nominal
Tx Disable Assert Time	toff_txdis	400	ms	Time from Tx Disable bit set cleared (value = 0b)[1] until optical output rises above 90% of nominal
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit set cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Desassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.
ModSelL Setup Time	Host_select_setup	2	ms	Setup time on select line before start of a host initiated serial bus sequence
ModSelL Hold Time	Host_select_hold	10	ms	Delay from completion of a serial bus sequence to change of Module select status
Aborted sequence - bus release	Deselect_Abort	2	ms	Delay from a host de-assertion ModSelL (at any point in a bus sequence) to the COBO Module releasing SCL and SDA

Table 2-7: I/O Timing For Squelch and Disable

Note 1: Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.

2.5 Power Supply

This section describes the power supply and return path specifications.

2.5.1 OBO Hot Pluggability

The OBO does not support hot pluggability.

2.5.2 OBO Power Supply Noise Output

The OBO shall generate less than the value specified in Table 2-8 when tested by the methods of SFF-8431, section D.17.2. Note: The series resister specified in D.17 Figure 56 may need to be reduced for high power OBOs.

2.5.3 OBO Power Supply Noise Tolerance

The OBO shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 2-8, swept from 10Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst-case noise output of the host.

2.5.4 Return Path Isolation

For the 16-lane application, the host return path does not require isolation between the two 8 lane connectors. It is up to the host PCB to keep the noise contributions within the limit of the OBO requirements.

2.5.5 OBO Power Sequencing

No power sequencing is required for the OBO.

2.5.6 OBO Power Supplies Requirements

The host board power supply is responsible for supplying up to the maximum current limits during startup.

Parameters	Symbol	Min	Nom	Max	Unit	Notes
Host power supply voltages including ripple, droop and noise	VCC	3.14	3.30	3.47	V	<100kHz
Power Consumption, operating 8Lane 16Lane	POP			 20.8 41.6	 W W	See Note 1 & 2
Power Consumption, Low power mode 8Lane 16Lane	PLP			 1.5 3	 W W	
Low-Speed connector current per pin (2)				1.5	A	Including deratings
High-Speed connector current per pin				0.9	A	Including deratings
Host RMS noise output				25	mV	10Hz -10MHz, See SFF-8419. A.1.1
OBO RMS Noise output				15	mV	10Hz -10MHz, See SFF-8419. A.1.2.
OBO Power Supply Tolerance				66	mV (p-p)	10Hz -10MHz See SFF-8419. A.1.3.

Table 2-8: Power Supply Requirements

Note 1. The OBOs power classes described in the CMIS, “Module Card Power Class” register (200h), are not used and instead, the host relies on the value populated in the “Max Power” register (201h).

Note 2. Two additional pins are available on the low-speed connector and are targeted “For Future Use” (FFU). In the event these pins are assigned as power supply pins, the current carrying capacity of the power pins is reduced to 1.4A per pin. If these pins are assigned to a 3.3V supply, the max operating power consumption of the OBO increases to 29.1W.

2.5.7 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 2-8 when tested by the methods of SFF-8431, section D.17.1.

2.6 Management Interface Specifications

A 2-wire interface, TWI, is specified to enable the OBO by the user. The OBO TWI specifications are based on the SFF-8636, see SNIA repository, with the difference to support 8 and 16 channels hence not backwards compatible with SFF-8636.

The OBO memory map applications register mapping is the Common Management Interface Specifications, CMIS.

For more information see CMIS latest revision.

2.6 TWI Timing Specifications

The TWI consists of a SCL (Clock) and SDA (Data) signals. The interface is based on Low Voltage CMOS (LVC-MOS) operating at VCC. See SFF-8679 Subsection 5.3 for more details. Nomenclature for all registers more than 1 bit long is MSB-LSB.

The TWI timing parameters are shown on Figure 2-13 and specifications in Table 2-9.

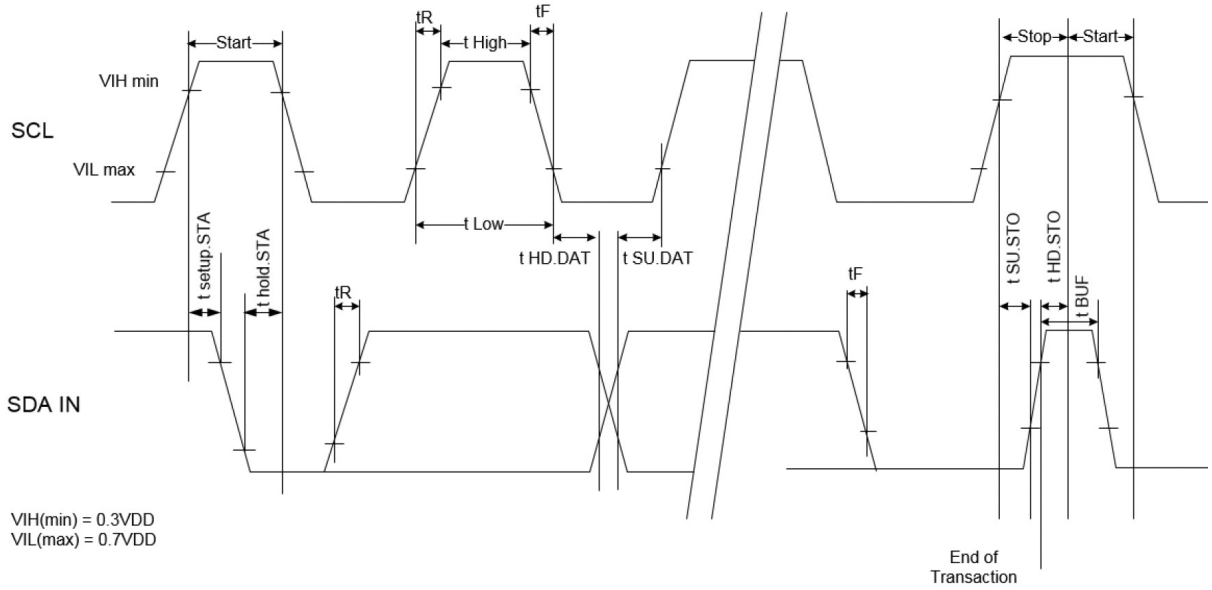


Table 2-13: TWI Timing Diagram

Parameter	Symbol	Conditions	Fast Mode		Fast Mode-Plus		Unit
			Min	Max	Min	Max	
SCL clock frequency	fSCL			400		1000	kHz
Clock period width - Low	tLOW		1.3		0.5		µs
Clock period width - High	tHIGH		0.6		0.26		µs
Time bus free before new transmission can start	tBUF	Between STOP and START and between ACK and ReStart	20		1		µs

Table 2-9: TWI Management Interface Specifications

Parameter	Symbol	Conditions	Fast Mode		Fast Mode-Plus		Unit
			Min	Max	Min	Max	
Start Hold time	tHD.STA	The delay required between SDA becoming low and SCL starting to go low in a START	0.6		0.26		µs
Start Setup Time	tSU.STA	The delay required between SCL becoming high and SDA starting to go low in a START	0.6		0.26		µs
Data In Hold Time	tHD.DAT		0		0		µs
Data In Setup Time	tSU.DAT		0.1		0.1		µs
Input Rise Time	tR	From (VIL, MIN+0.15) to (VIH, MAX-0.15)		300		120	ns
Input Fall Time	tF	From (VIH, MIN+0.15) to (VIL, MAX-0.15)		300		120	ns
STOP Setup Time	tSU.STO		0.6		0.6		µs
STOP Hold Time	tHD.STO		0.6		0.6		µs
Aborted sequence — bus release	Deselect _Abort	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the OBO module releasing SCL and SDA	2		2		ms
ModSelL Setup Time - See Note 1	tSU.ModSelL	ModSelL Setup Time is the setup time on the select lines before the start of a host initiated serial bus sequence	2		2		ms
ModSelL Hold Time- See Note 1	tHD.ModSelL	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of OBO Select status	2		2		ms
Serial Interface Clock Holdoff "Clock Stretching"	T Clock hold	Maximum time the OBO may hold the SCL line low before continuing with a read or write operation		500		500	µs
Complete Single or Sequential Write	tWR	Complete (up to) 4 Byte Write		40		40	ms
Endurance (Write Cycles)		OBO Case Temperature = 70 C	50k			50k	Cycles

Table 2-9: TWI Management Interface Specifications (cont')

Note 1. When the host has determined that module is OBO, the management registers can be read to determine alternate supported ModSelL set up and hold times.

3.0 Optical Connectivity

3.1 Purpose

Optical signals need to be transmitted from the OBO to the panel (e.g. card edge, faceplate, backplane). Optical fiber is the recognized medium for high-speed, low-loss signal transmission. This section explains the normative requirements that will underlie yet-to-be-determined industry-standard COBO link definition and test requirements.

3.2 Scope

This section includes the following normative requirements:

- Definitions of the PMD, MDI, TP2, and TP3 per IEEE 802.3bs 400Gb/s Ethernet standard
- Defined test points along the link
- Fiber optic connectors at the MDI
- Fiber optic lane assignments at the MDI

3.3 COBO Optical Link Convention

To create a sustainable OBO ecosystem, there must be a clear, consistent definition of the OBO and the optical link, including all relevant test points.

3.3.1 COBO On-Board Optic

The COBO standard follows the IEEE convention of an optical module. Since most existing industry standards and/or MSAs assume the use of pluggable optical modules, it is important to properly define the conventions and test point locations specific to OBOs. Figure 3-1 illustrates and defines this for both pigtailed and connectorized OBOs. Both formats would typically be designed and manufactured by the transceiver manufacturer, with input from their fiber and connector suppliers. The PMD is the portion of the device which gets attached onto the PCBA. The MDI location is where the transceiver manufacturer measures the optical performance of the PMD according to the standard.

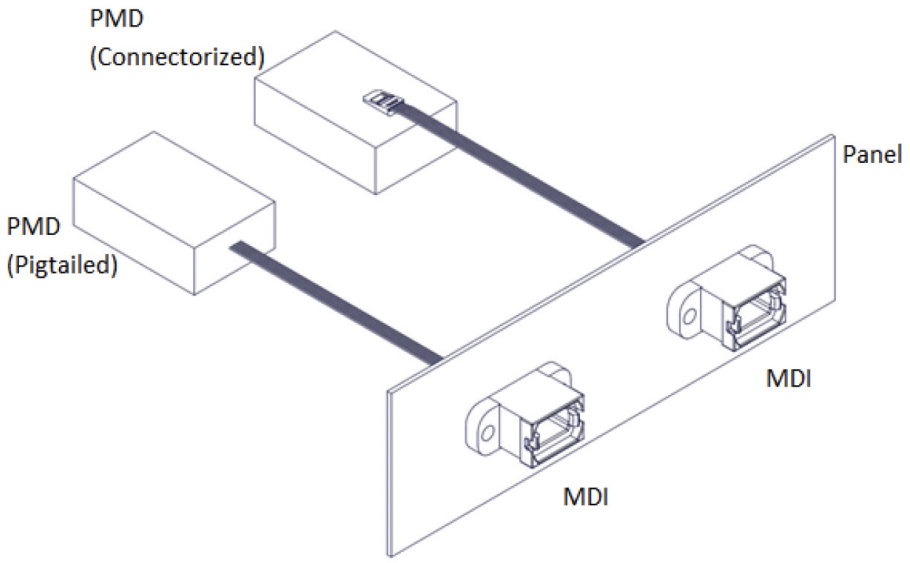


Figure 3-1: IEEE PMD & MDI Defined Locations For Pigtailed and Connectorized OBOs

3.3.2 COBO Optical Link

The COBO standard also follows the IEEE convention for an entire optical link. In addition to the PMD and MDI terms above, it leverages the IEEE 802.3bs definitions of TP2, and TP3. Figure 3-2a shows a pluggable optical module (i.e. not an OBO) for reference. Figure 3-2b and Figure 3-2c defines the proper convention for pigtailed and connectorized OBOs respectively. TP2 is typically where the systems maker and/or end user measures the output power of the source PMD. It is measured at the end of a fiber optic patch cord that is connected to the MDI. Similarly, TP3 is typically where the systems maker and/or end user measures the receive signal going into the MDI of the destination PMD. In between the two MDI points, there can be a significant amount of passive infrastructure that routes/aggregates all the fiber. Since the COBO standard is not specific to any one application, the term "Data Center Cabling" can represent any such infrastructure (ranging from simple point-to-point to more complex structured cabling).

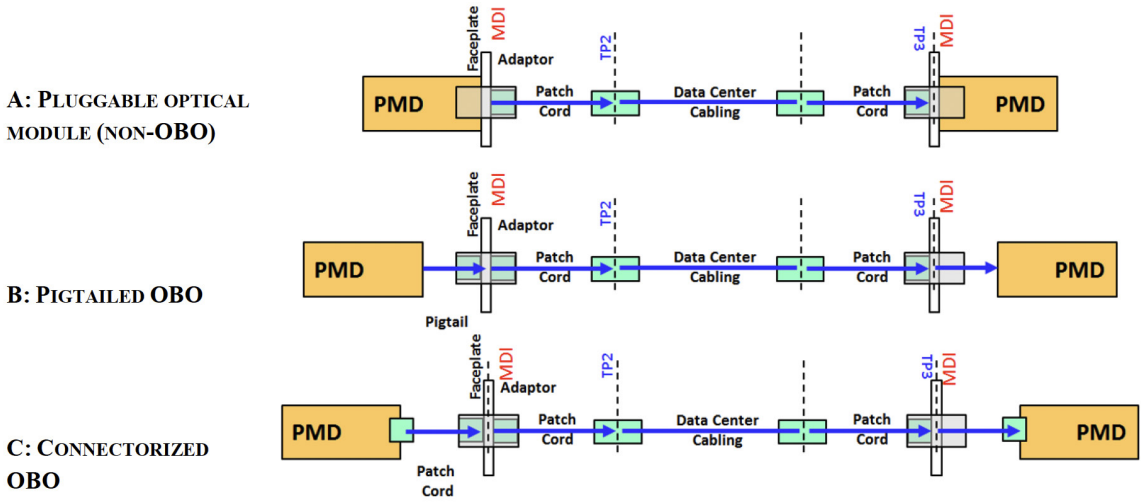


Figure 3-2: COBO Convention Based on IEEE Definitions

3.4 Fiber Optic Connectors at the MDI

The fiber optic connector used at the MDI is primarily dependent on fiber count. In general, PMDs that use more than two fibers are best served by using a multi-fiber connector. Fiber optic connectors as described in §3.4.1-§3.4.3, shall meet the industry standards for mechanical intermateability, as well as the lane assignment requirements defined in §3.5. Other connector types with similar fiber count may be considered as long as they meet the lane assignment requirements defined in §3.5.

3.4.1 MPO Optical Cable Connections

The optical plug and receptacle for the MPO-12 connector is specified in TIA-604-5 or in IEC 61754-7-1 (one fibre row) and IEC 61754-7-2 (two fibre rows) and shown in Figure 3-3 (MPO-12 Single Row) and Figure 3-4 (MPO-12 Two Row). Note: This specification sometimes uses the terms "MPO-12" and "MPO-12 Two Row" in place of the TIA terms "MPO" and "MPO Two Row," respectively.

The optical plug and receptacle for the MPO-16 connector is specified in TIA-604-18 or in IEC 61754-7-4 (one fibre row) and IEC 61754-7-3 (two fibre rows) and shown in Figure 3-5 (MPO-16 Single Row) and Figure 3-6 (MPO-16 Two Row).

Both MPO and MPO-16 OBOs use aligned keys to ensure alignment at the MDI between the OBO and the patch cord. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

Note: Two alignment pins are fixed in each device receptacle. This is commonly referred to as the “male” side of the connection.

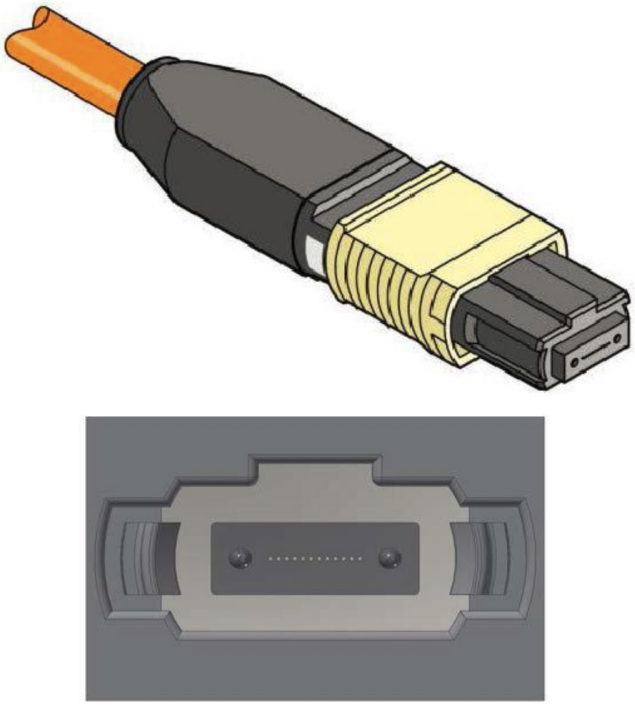


Figure 3-3: MPO-12 Single Row Optical Patch Cord and OBO Receptacle

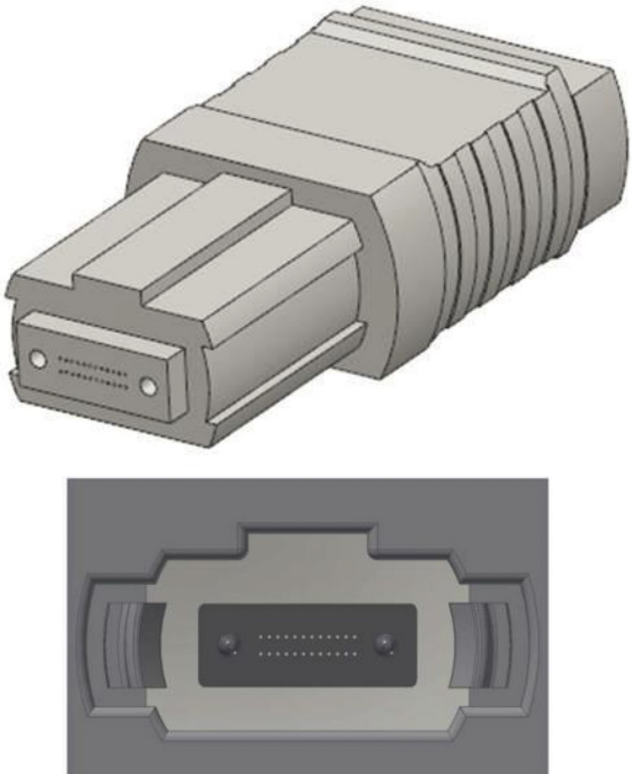


Figure 3-4: MPO-12 Two Row Optical Patch Cord and OBO Receptacle

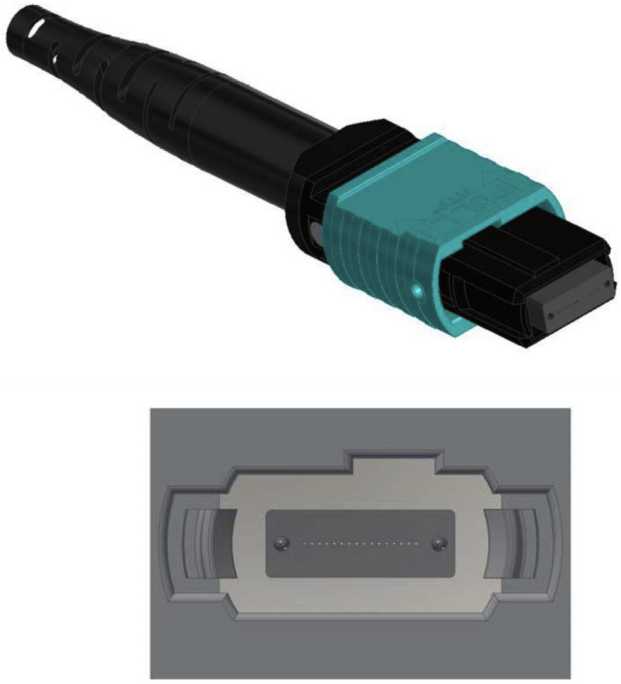


Figure 3-5: MPO-16 Single Row Optical Patch Cord and OBO Receptacle

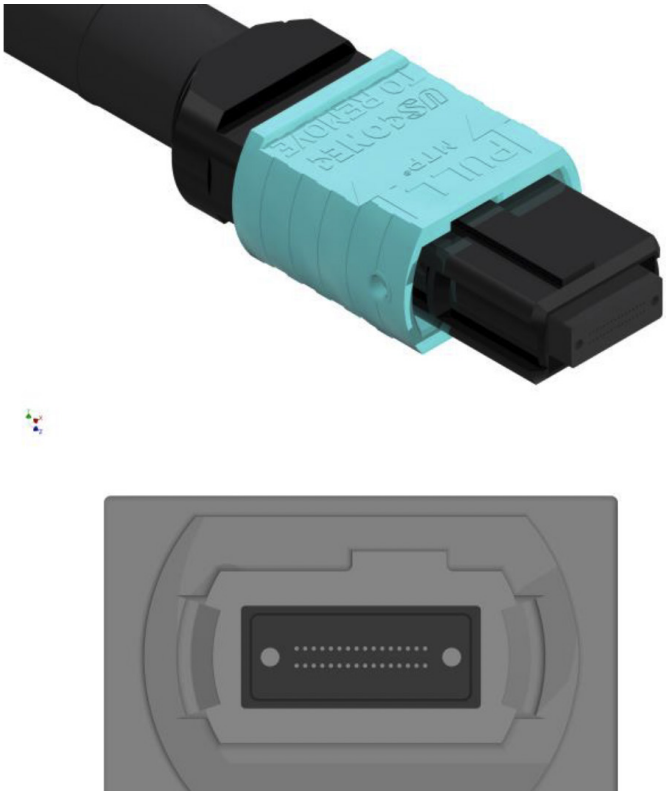


Figure 3-6: MPO-16 Two Row Optical Patch Cord and OBO Receptacle

3.4.2 Dual LC Optical Cable Connection

The Dual LC optical patch cord and OBO receptacle is specified in TIA-604-10 or in IEC-61754-20 and shown in Figure 3-7.

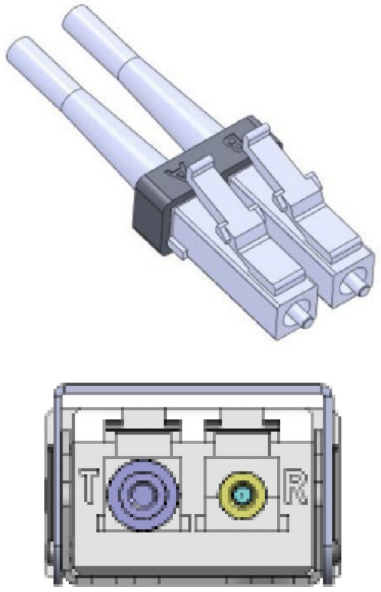


Figure 3-7: Dual LC Optical Patch Cord and OBO Receptacle

3.4.3 CS Optical Cable Connection

The CS optical patch cord and receptacle is shown in Figure 3-8. At the time of the COBO standard, this connector is in the process of being standardized. More information can be found at: http://www.qsfp-dd.com/

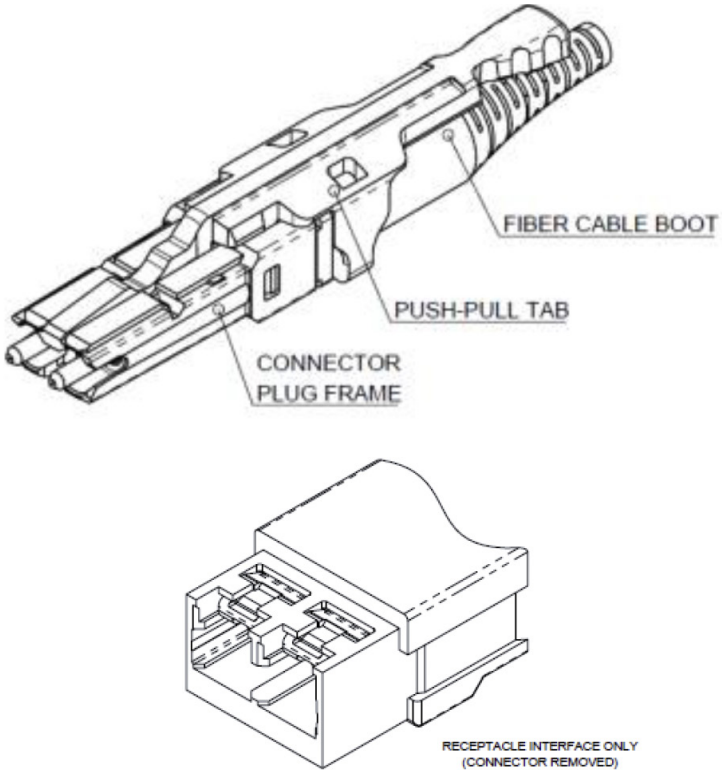
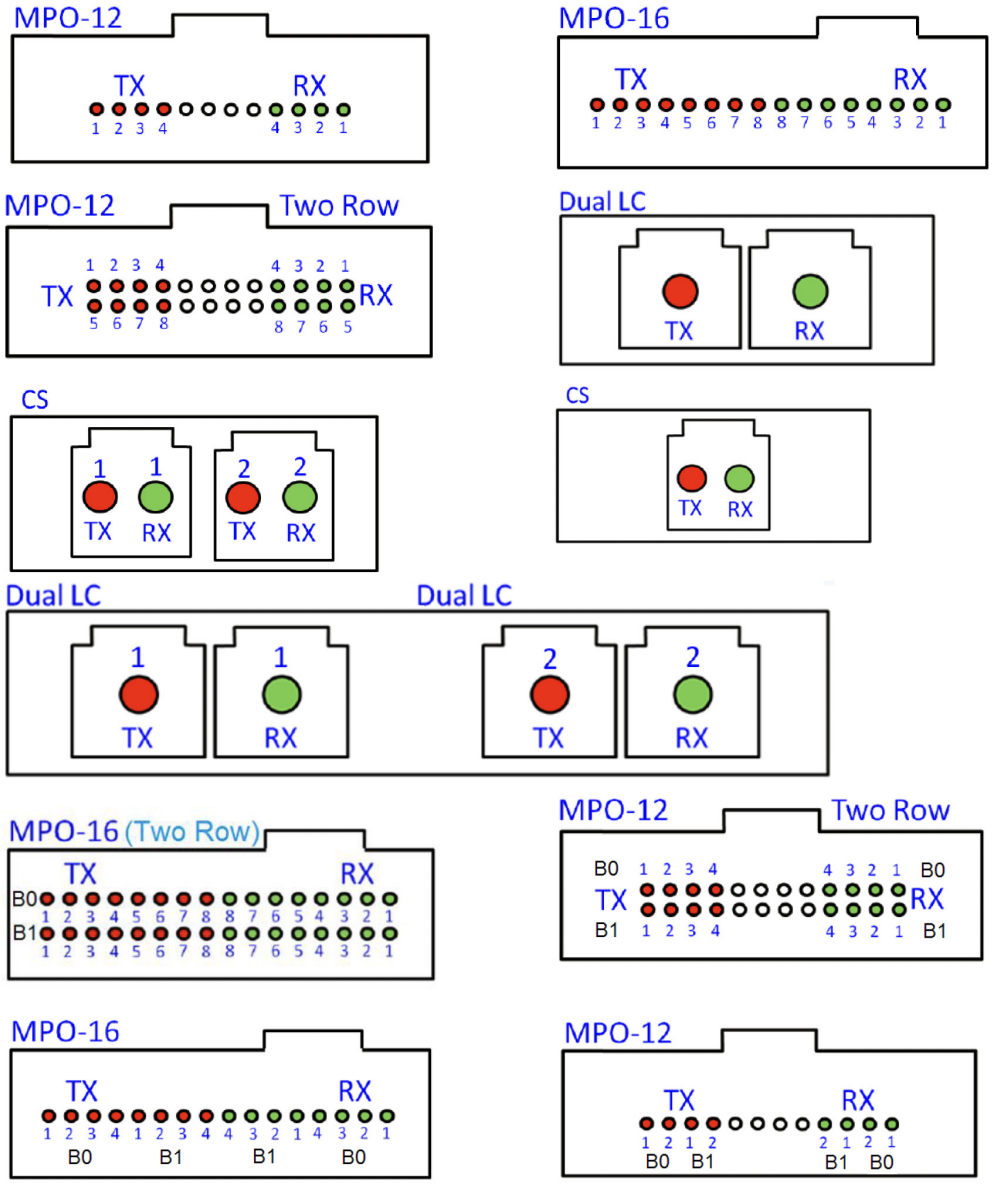


Figure 3-8: CS Optical Patch Cord and OBO Receptacle

3.5 Fiber Optic Lane Assignments at the MDI

When the optical interface port is a male MPO (Figure 3-3 & Figure 3-4), a male MPO-16 (Figure 3-5 & Figure 3-6), a dual LC (Figure 3-7), or a CS (Figure 3-8) connector receptacle, the recommended location and numbering of the optical lanes for the MDI is shown in Figure 3-9. The transmit and receive optical lanes shall occupy the positions depicted in Figure 3-9 when looking into the MDI receptacle, from outside the panel, and with the connector keyway feature on top. These same assignments shall be used if the OBO is connectorized with any of these optical interface ports. Other connector types with similar fiber count and arrangement shall adhere to these same assignments.



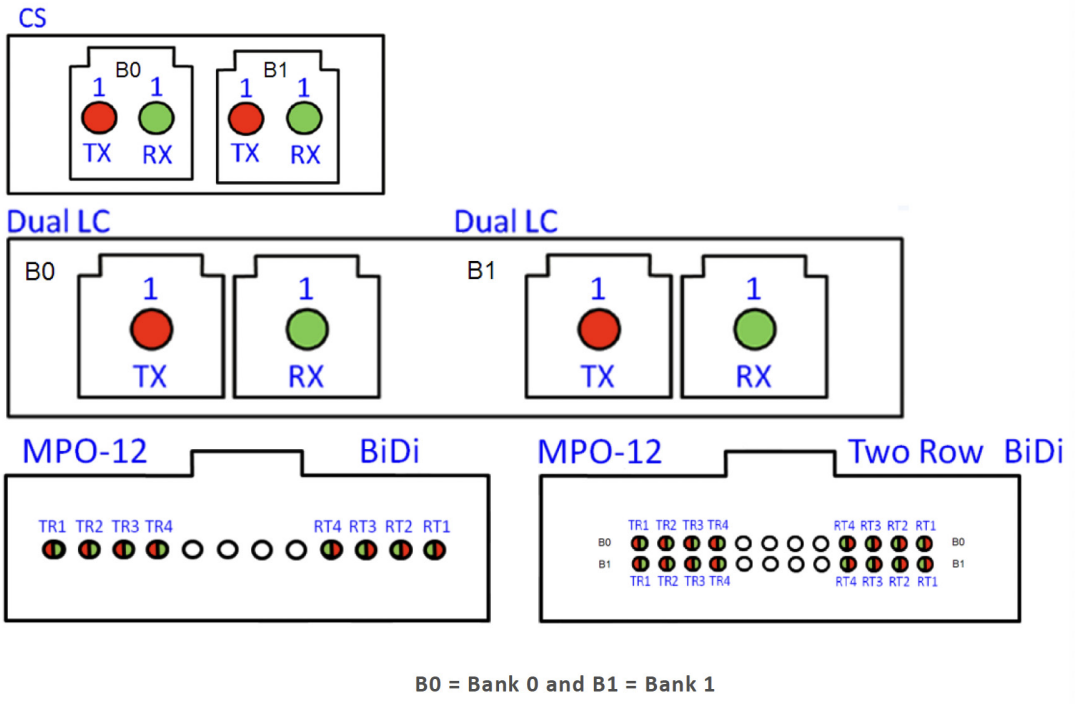


Figure 3-9: Fiber Optic Lane Assignments at MDI

Source: Artwork adapted from QSFP-DD MSA Specification.

3.5.1 Electrical data input/output to optical port mapping

Table 3-1 and Table 3-2 define the mapping of electrical TX data inputs to optical ports. The mapping of the RX optical ports to electrical RX outputs is symmetric. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

Electrical Signal	Optical Port Type (See Figure 3-3)				
	Dual-LC or CS	Dual-LC or CS or MPO-12	MPO-12	MPO-12 (Two Row) or MPO-16	MPO-12 BiDi
	1 TX Fiber	2 TX Fibers	4 TX Fibers	8 TX Fibers	8 TX (RX) Fibers[2]
	1 RX Fiber[1]	2 RX Fibers[1]	4 RX Fibers[1]	8 RX Fibers[1]	
Tx1	TX-1	TX-1	TX-1	TX-1	TR1
Tx2				TX-2	RT1
Tx3			TX-2	TX-3	TR2
Tx4				TX-4	RT2
Tx5		TX-2	TX-3	TX-5	TR3
Tx6				TX-6	RT3
Tx7			TX-4	TX-7	TR4
Tx8				TX-8	RT4
Rx1	RX-1	RX-1	RX-1	RX-1	RT1
Rx2				RX-2	TR1
Rx3			RX-2	RX-3	RT2
Rx4				RX-4	TR2
Rx5		RX-2	RX-3	RX-5	RT3
Rx6				RX-6	TR3
Rx7			RX-4	RX-7	RT4
Rx8				RX-8	TR4
Note 1: TX-n or RX-n, where n is the optical port number as defined in the Figure 3-3.					
Note 2: TRn or RTn where n is the optical port number as defined in Figure 3-3.					

Table 3-1: Electrical Signal to Optical Port Mapping for 8-Lane OBOs (x8)

Electrical Signal	Optical Port Type (See Figure 3-3)									
	Bank 1					Bank 0 and Bank 1 Combined				
	Dual-LC or CS	Dual-LC or CS or MPO-12	MPO-12	MPO-12 (Two Row) or MPO-16	MPO-12 BiDi	Dual-LC or CS or MPO-12	MPO-12	MPO-12 (Two Row) or MPO-16	MPO-16 (Two Row)	MPO-12 (Two Row) BiDi
	1 TX & 1 RX Fiber[1]	2 TX & 2 RX Fibers[1]	4 TX & 4 RX Fibers[1]	8 TX & 8 RX Fibers[1]	8 TX (RX) Fibers[2]	2 TX & 2 RX Fibers[1]	4 TX & 4 RX Fibers[1]	8 TX & 8 RX Fibers[1]	16 TX & 16 RX Fibers[1]	16 TX (RX) Fibers[2]
Tx1_1	B1_TX-1	B1_TX-1	B1_TX-1	B1_TX-1	B1_TR1	B1_TX-1	B1_TX-1	B1_TX-1	B1_TX-1	B1_TR1
Tx2_1				B1_TX-2	B1_RT1				B1_TX-2	B1_RT1
Tx3_1			B1_TX-2	B1_TX-3	B1_TR2			B1_TX-2	B1_TX-3	B1_TR2
Tx4_1				B1_TX-4	B1_RT2				B1_TX-4	B1_RT2
Tx5_1		B1_TX-2	B1_TX-3	B1_TX-5	B1_TR3		B1_TX-2	B1_TX-3	B1_TX-5	B1_TR3
Tx6_1				B1_TX-6	B1_RT3				B1_TX-6	B1_RT3
Tx7_1			B1_TX-4	B1_TX-7	B1_TR4			B1_TX-4	B1_TX-7	B1_TR4
Tx8_1				B1_TX-8	B1_RT4				B1_TX-8	B1_RT4
Rx1_1	B1_RX-1	B1_RX-1	B1_RX-1	B1_RX-1	B1_RT1	B1_RX-1	B1_RX-1	B1_RX-1	B1_RX-1	B1_RT1
Rx2_1				B1_RX-2	B1_TR1				B1_RX-2	B1_TR1
Rx3_1			B1_RX-2	B1_RX-3	B1_RT2			B1_RX-2	B1_RX-3	B1_RT2
Rx4_1				B1_RX-4	B1_TR2				B1_RX-4	B1_TR2
Rx5_1		B1_RX-2	B1_RX-3	B1_RX-5	B1_RT3		B1_RX-2	B1_RX-3	B1_RX-5	B1_RT3
Rx6_1				B1_RX-6	B1_TR3				B1_RX-6	B1_TR3
Rx7_1			B1_RX-4	B1_RX-7	B1_RT4			B1_RX-4	B1_RX-7	B1_RT4
Rx8_1				B1_RX-8	B1_TR4				B1_RX-8	B1_TR4

Note 1: B0_TX-n or B1_TX-n and B0_RX-n or B1_RX-n, where n is the optical port number as defined in the Figure 3-3.

Note 2: B0_TRn or B0_RTn and B1_TRn or B1_RTn where n is the optical port number as defined in Figure 3-3.

Electrical Signal	Bank 0									
	Dual-LC or CS	Dual-LC or CS or MPO-12	MPO-12	MPO-12 (Two Row) or MPO-16	MPO-12 BiDi					
	1 TX & 1 RX Fiber[1]	2 TX & 2 RX Fibers[1]	4 TX & 4 RX Fibers[1]	8 TX & 8 RX Fibers[1]	8 TX (RX) Fibers[2]					
Tx1	B0_TX-1	B0_TX-1	B0_TX-1	B0_TX-1	B0_TR1	B0_TX-1	B0_TX-1	B0_TX-1	B0_TX-1	B0_TR1
Tx2				B0_TX-2	B0_RT1				B0_TX-2	B0_RT1
Tx3			B0_TX-2	B0_TX-3	B0_TR2			B0_TX-2	B0_TX-3	B0_TR2
Tx4				B0_TX-4	B0_RT2				B0_TX-4	B0_RT2
Tx5		B0_TX-2	B0_TX-3	B0_TX-5	B0_TR3		B0_TX-2	B0_TX-3	B0_TX-5	B0_TR3
Tx6				B0_TX-6	B0_RT3				B0_TX-6	B0_RT3
Tx7			B0_TX-4	B0_TX-7	B0_TR4			B0_TX-4	B0_TX-7	B0_TR4
Tx8				B0_TX-8	B0_RT4				B0_TX-8	B0_RT4
Rx1	B0_RX-1	B0_RX-1	B0_RX-1	B0_RX-1	B0_RT1	B0_RX-1	B0_RX-1	B0_RX-1	B0_RX-1	B0_RT1
Rx2				B0_RX-2	B0_TR1				B0_RX-2	B0_TR1
Rx3			B0_RX-2	B0_RX-3	B0_RT2			B0_RX-2	B0_RX-3	B0_RT2
Rx4				B0_RX-4	B0_TR2				B0_RX-4	B0_TR2
Rx5		B0_RX-2	B0_RX-3	B0_RX-5	B0_RT3		B0_RX-2	B0_RX-3	B0_RX-5	B0_RT3
Rx6				B0_RX-6	B0_TR3				B0_RX-6	B0_TR3
Rx7			B0_RX-4	B0_RX-7	B0_RT4			B0_RX-4	B0_RX-7	B0_RT4
Rx8				B0_RX-8	B0_TR4				B0_RX-8	B0_TR4

Note 1: B0_TX-n or B1_TX-n and B0_RX-n or B1_RX-n, where n is the optical port number as defined in the Figure 3-3.

Note 2: B0_TRn or B0_RTn and B1_TRn or B1_RTn where n is the optical port number as defined in Figure 3-3.

Table 3-2: Electrical Signal to Optical Port Mapping for 16-Lane OBOs (x16)

4.0 Mechnical

4.1 Introduction

The OBO connector system is ideal for the on-board optics application due to its flexibility, excellent signal integrity, and cost-effective design. It consists of a card-edge connector for the high-speed function and a one-piece z-axis connector for management interface and power contacts. Figure 4-1 shows the connector elements that make up this solution.

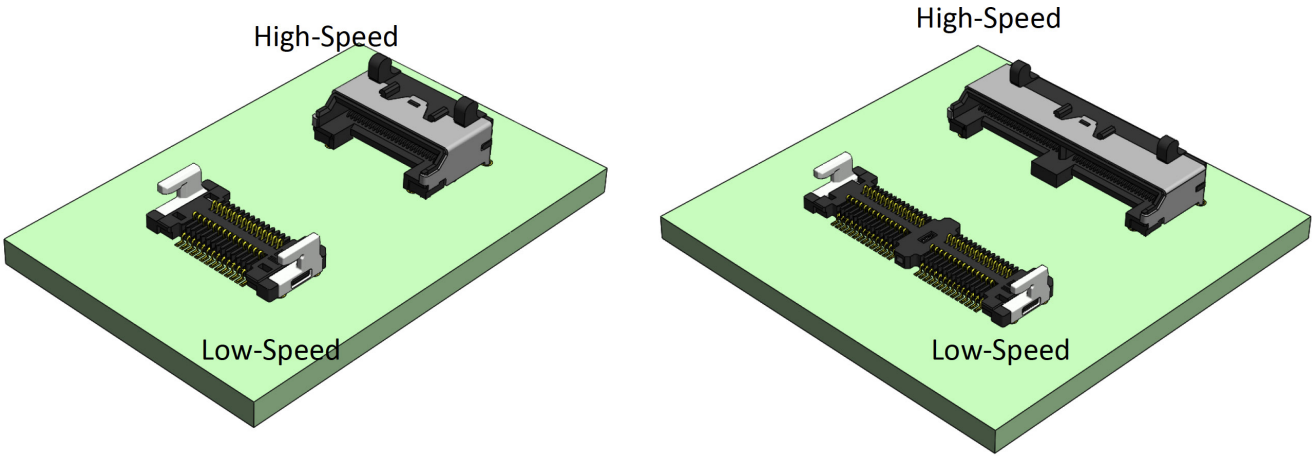


Figure 4-1: OBO Connector Elements

The high-speed card-edge connector is specified in two versions to support ×8 and ×16 channel requirements. The signal integrity (SI) performance of the connector system supports the COBO requirement of operation at 56Gbps PAM4 signaling. Additionally, it has been presented to the COBO working group that the connector interface is extendable in performance to 112Gbps PAM4 via a connector upgrade that will make it 56Gbps NRZ capable, which will support current industry efforts to define a higher-order modulation for 112Gbps PAM4 signaling, while fully supporting a backwards-capable mechanical mating interface. The connector design utilizes contacts on a 0.6mm pitch.

The separate management interface / power connector is based on a robust 0.8mm contact pitch connector system, which allows for enough current carrying capacity for the higher powered OBOs and, like the high-speed connector, is specified in two versions. This connector mates with the OBO PCB via a z-axis (downward) force and provides the means to retain the OBO PCB against the contacts.

The specified connectors include built-in mechanical attachment elements that are through-hole soldered to the host PCB so that the connector system holds the OBO and associated heat sink to the host for all required mechanical environments, eliminating the need for additional holes and mechanisms for OBO retention.

A key feature of the connector system is its support of safe blind mating, needed when the OBO has a pre-attached heat sink whose size obscures the assembler's view of the mating connector. A heat sink over hanging the side of the OBO, and surrounding connectors already populated with OBO obscures the operator's view. As described later in this document, the connectors include features to reduce the risk of a non-aligned OBO damaging connector contacts or the OBO card edge interface.

This OBO connector system positions the OBO approximately 2.2mm above the host PCB so that low-profile components can be placed on the bottom of the OBO as well as OBO packaging elements which may be necessary for shielding and EMI management while at the same time not wasting space by having the OBO too high above the host PCB.

The OBO connector system requires a nominal 1.57mm thick PCB, providing a rugged and cost effective solution. This provides a robust mechanical substrate as the basis for the OBO while providing for routing layers that are anticipated for a 2×400 GbE OBO.

For each of the ×8 and ×16 channel version of connectors, there are three OBO form factors, Class A, Class B and Class C. These three form factors allow COBO to address various optical technologies, optical reaches and power-dissipation classes. The following illustration identifies the use cases; which OBOs can be used on which host implementations. The image shows the ×8 OBO/host examples and the same methodology and use cases apply to the ×16 OBO/host.

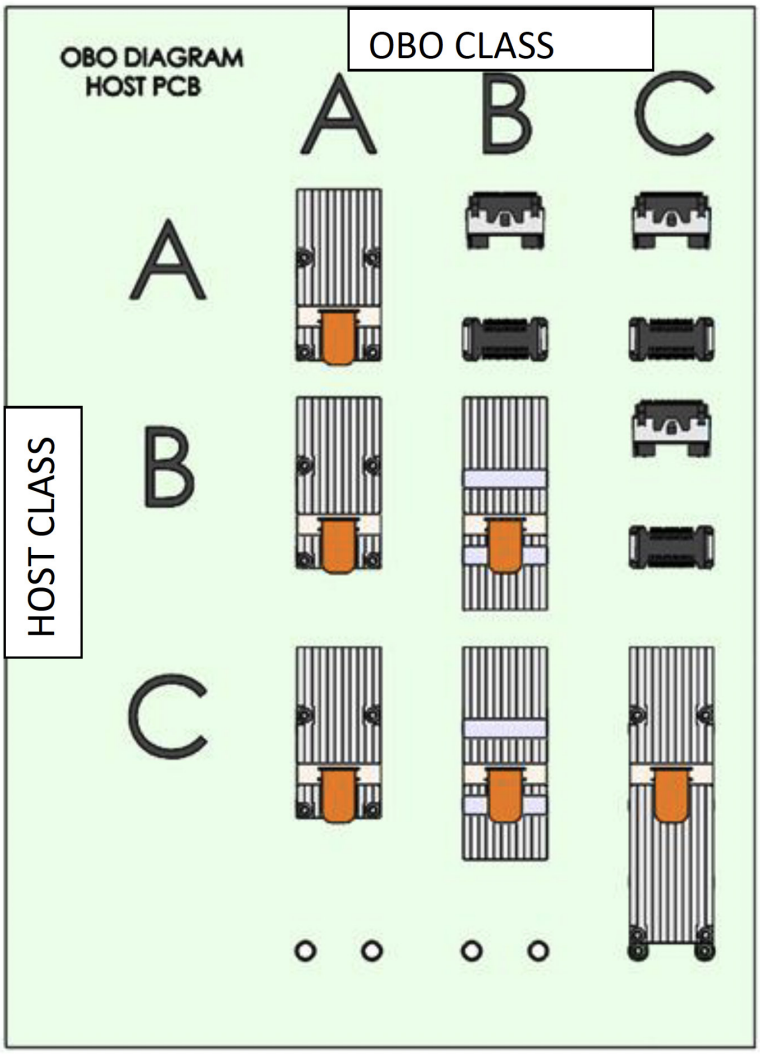


Figure 4-2: Host-OBO Class Compatability Chart

4.2 Mechanical specification

4.2.1 ×8 Solution

This section provides the mechanical details of the ×8 OBO (400G) interconnect solution; the ×8 OBO form factors (classes A, B, and C), host footprints, and mating application between the host connectors and the OBO. The ×8 form factors all utilize a two-electrical-connector solution for mounting to the host PCB. The electrical connectors used for all three OBO sizes are common to all three applications. The ×8 OBO is sized so that at least 32 OBOs can be fit into a 1RU equipment form factor. The OBO definition includes features to enable heat sink attachment to the OBOs by two methods.

4.2.1.1 ×8 OBO

The ×8 OBO is specified in 3 sizes - classes A, B, and C - to enable use with multiple optical technologies and optical reach specifications. The primary difference between the three form factors is OBO length. See Figure 4-3.

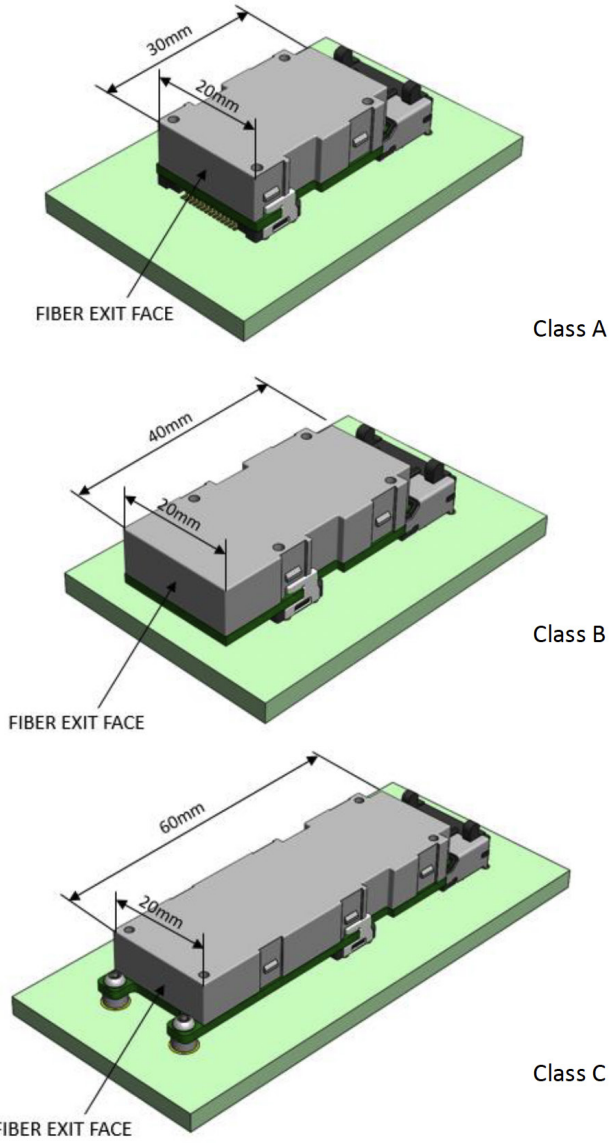


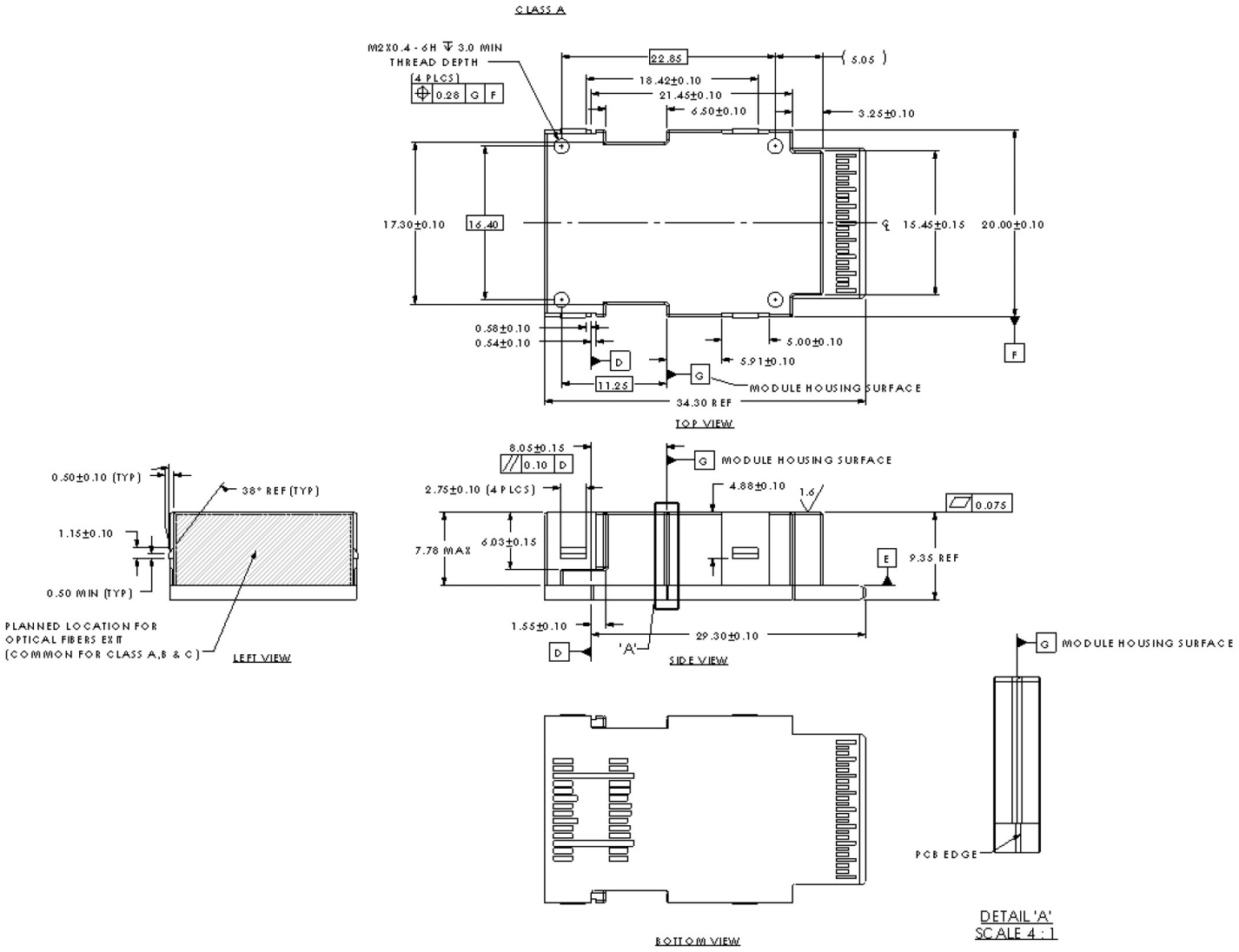
Figure 4-3: 8-Lane OBO Form Factor - Class A, B, and C

The datum structure used for the x8 OBO is identified in Table 4-1.

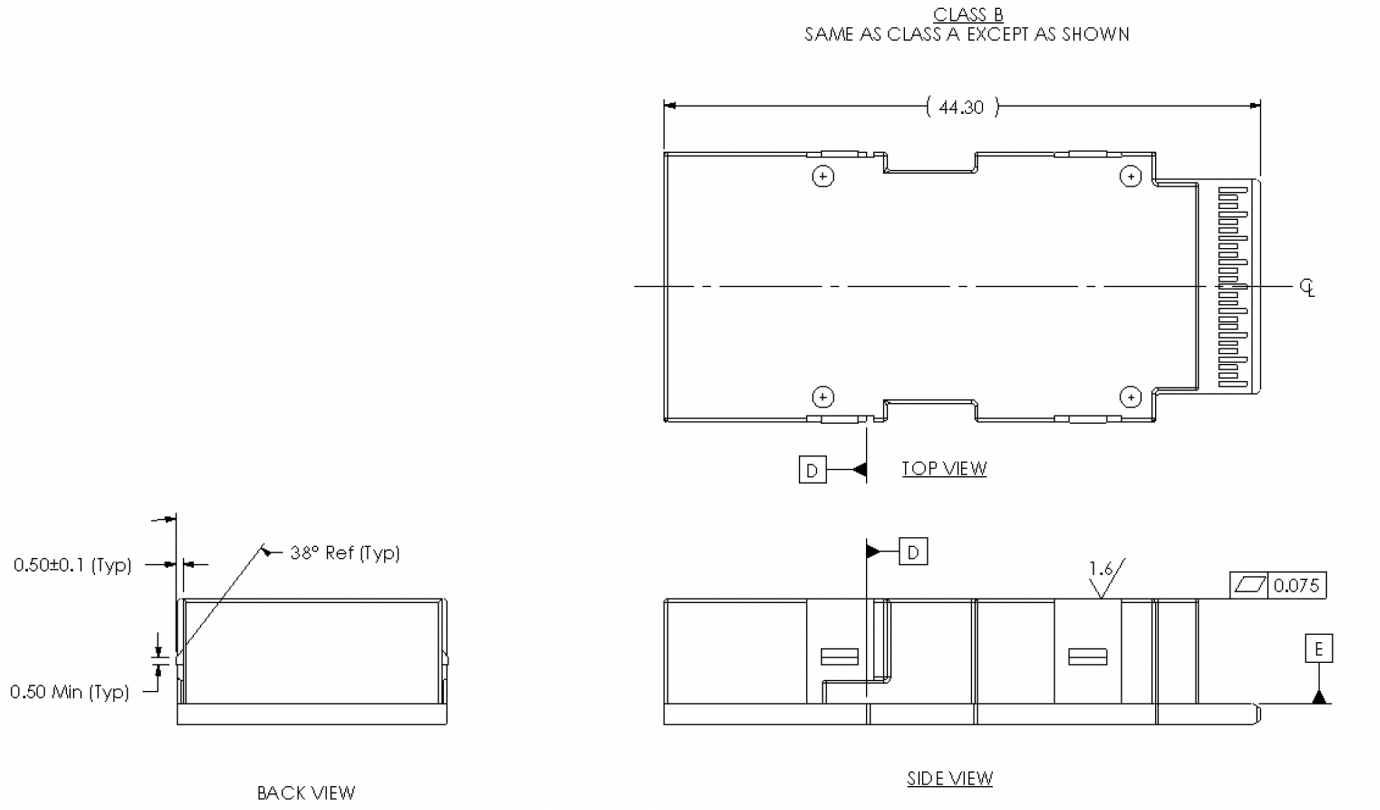
Datum	Description
A	Host board thru hole to accept high-speed connector guide post
B	Host board thru hole to accept low-speed connector guide post
D	Hard Stop on Low-Speed Connector
E	Bottom Surface of OBO Housing
F	Centerline of Width of OBO
G	OBO Reference Surface for Latch to Low-Speed Connector
H	OBO Reference Surface for Latch to High-Speed Connector
J	High-Speed Connector Mating Interface with OBO PCB Pads
K	Low-Speed Connector Mating Interface with Row 1 OBO PCB Pads
L	Low-Speed Connector Mating Interface with Row 2 OBO PCB Pads
M	Centerline of Width of OBO PCB
N	Top Surface of OBO PCB

Table 4-1: Datum Structure Used for x8 OBO

The three OBO form factors, classes A, B, and C, are shown in Figure 4-4. The OBOs included threaded holes on the top surface for heat sink attachment, as well as latch features on the OBO sides for attaching heat sinks by a set of spring clips. These will be discussed further in a later section.



Class A



Class B

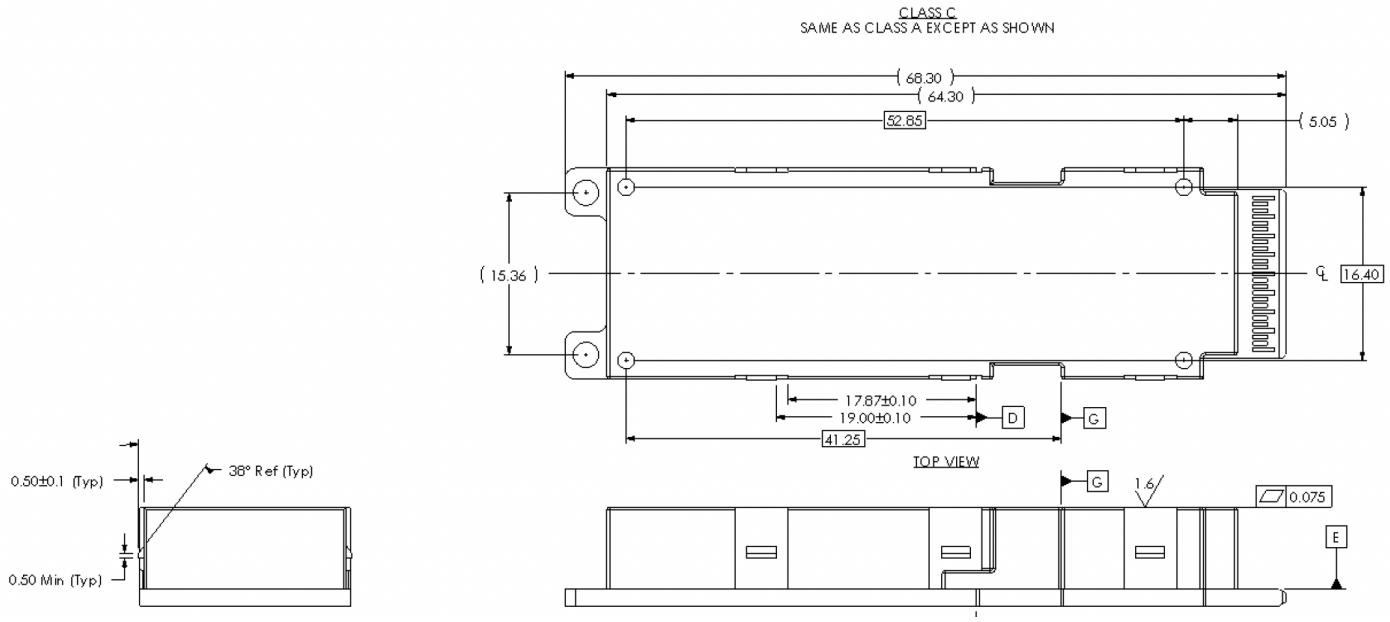
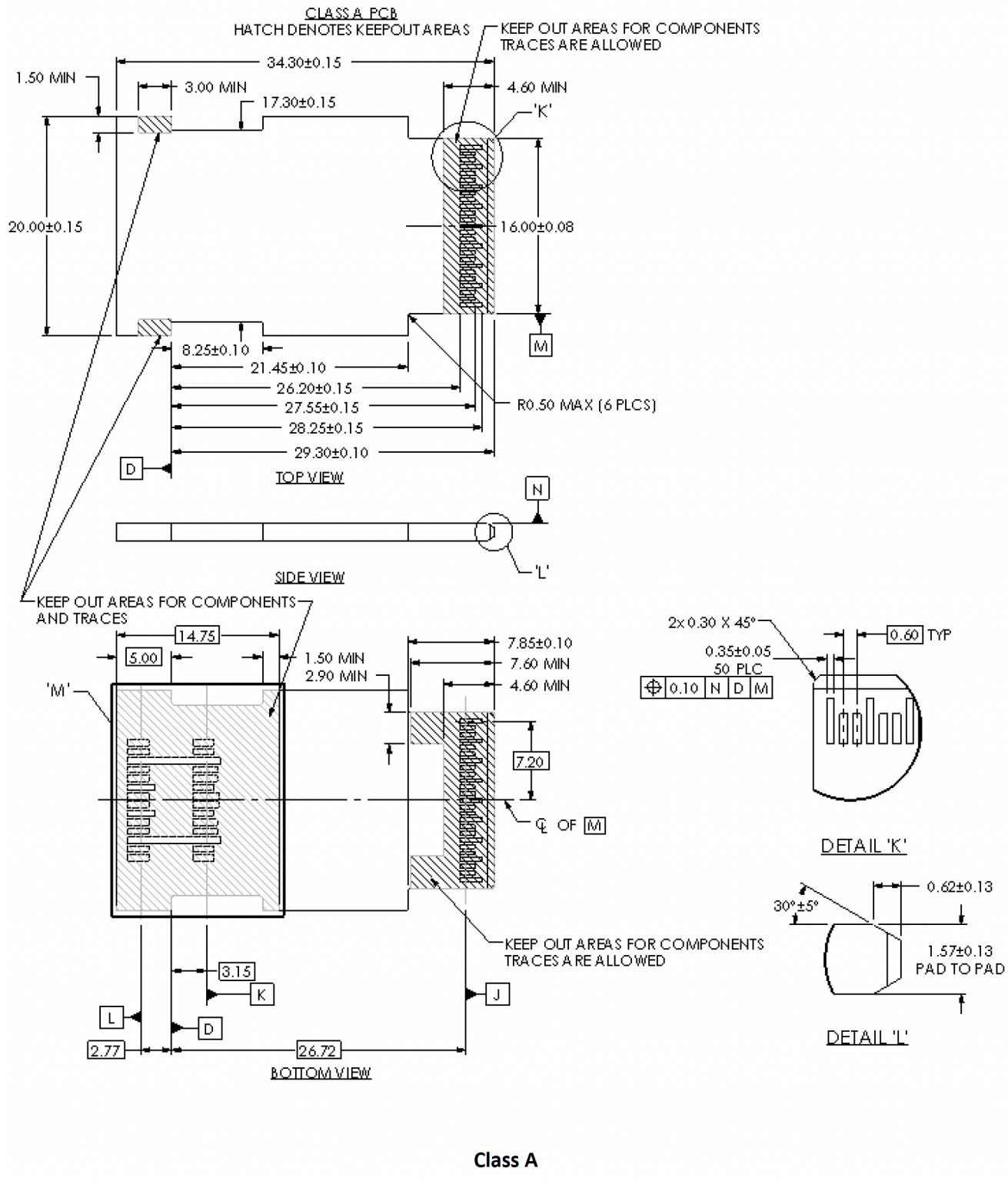
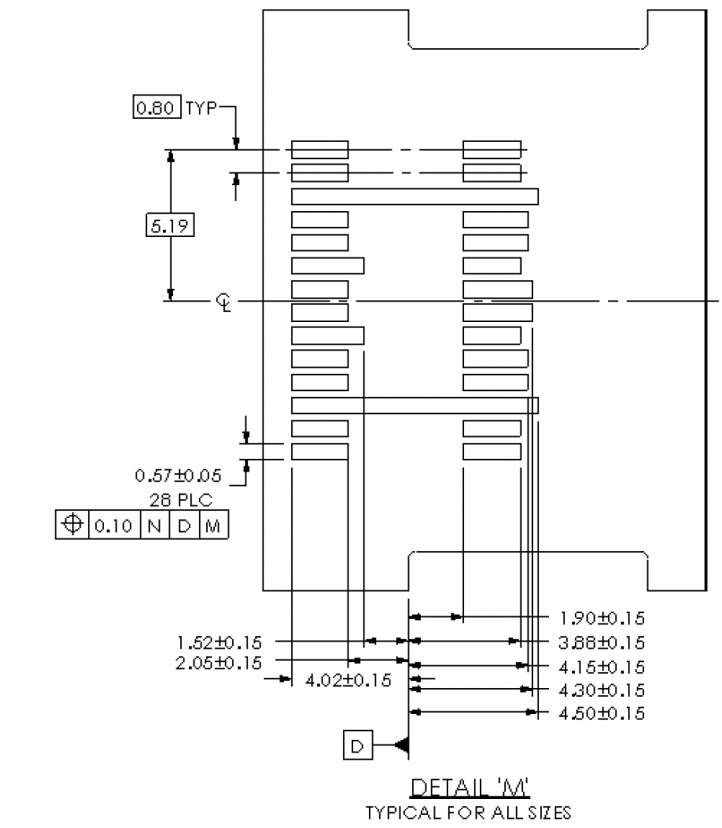


Figure 4-4: 8-Lane OBO Form Factor - Class A, B, and C

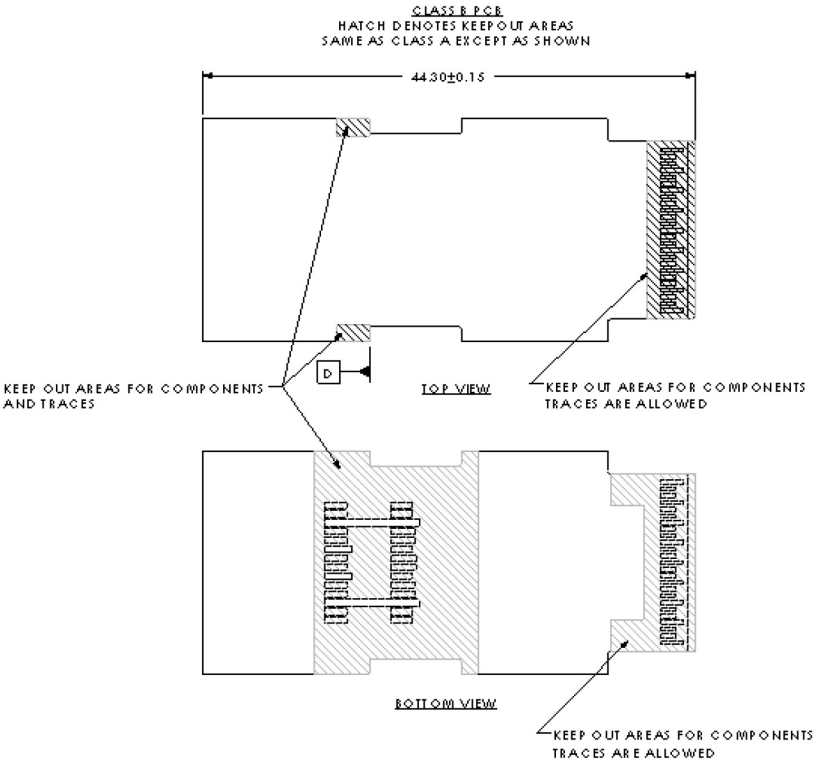
The OBO PCBs for the three form factors are shown in Figure 4-5.



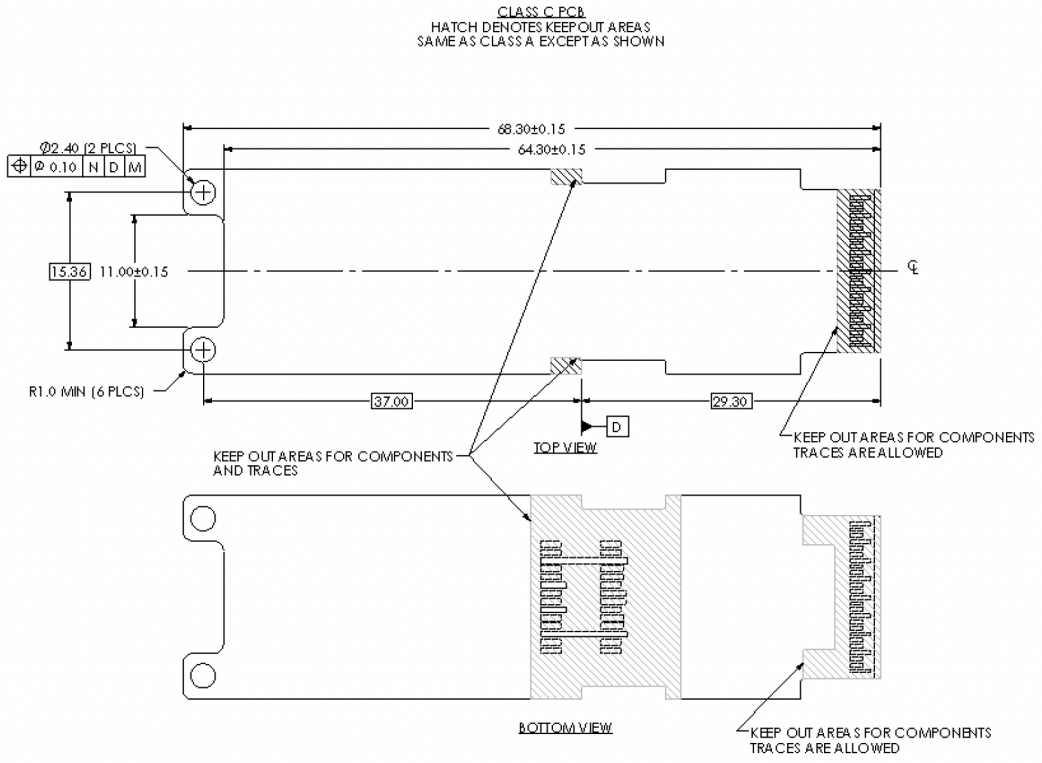
Class A



Class A, B, & C – Detail 'M'



Class B



Class C

Figure 4-5: 8-Lane OBO PCB - Class A, B, and C

4.2.1.2 ×8 Low-Speed connector

The ×8 Low-speed connector is an integrated assembly comprised of 28 contact positions on 0.8mm contact pitch. The low-speed connector functions by making z-axis contact with metalized pads on the bottom side of the OBO PCBs. The connector includes two integrated metal “J hook” features that engage the OBO and maintain the necessary clamping force between the OBO and connector. The low-speed connector also serves as the hard stop surface when the OBO is mating to the high-speed and low-speed connectors to prevent over insertion. The connector is applied with standard high-volume pick and place equipment. The power and signal contacts are attached via conventional SMT reflow soldering and the integrated hook features simultaneously attach to the host PCB using paste-in-hole soldering techniques.

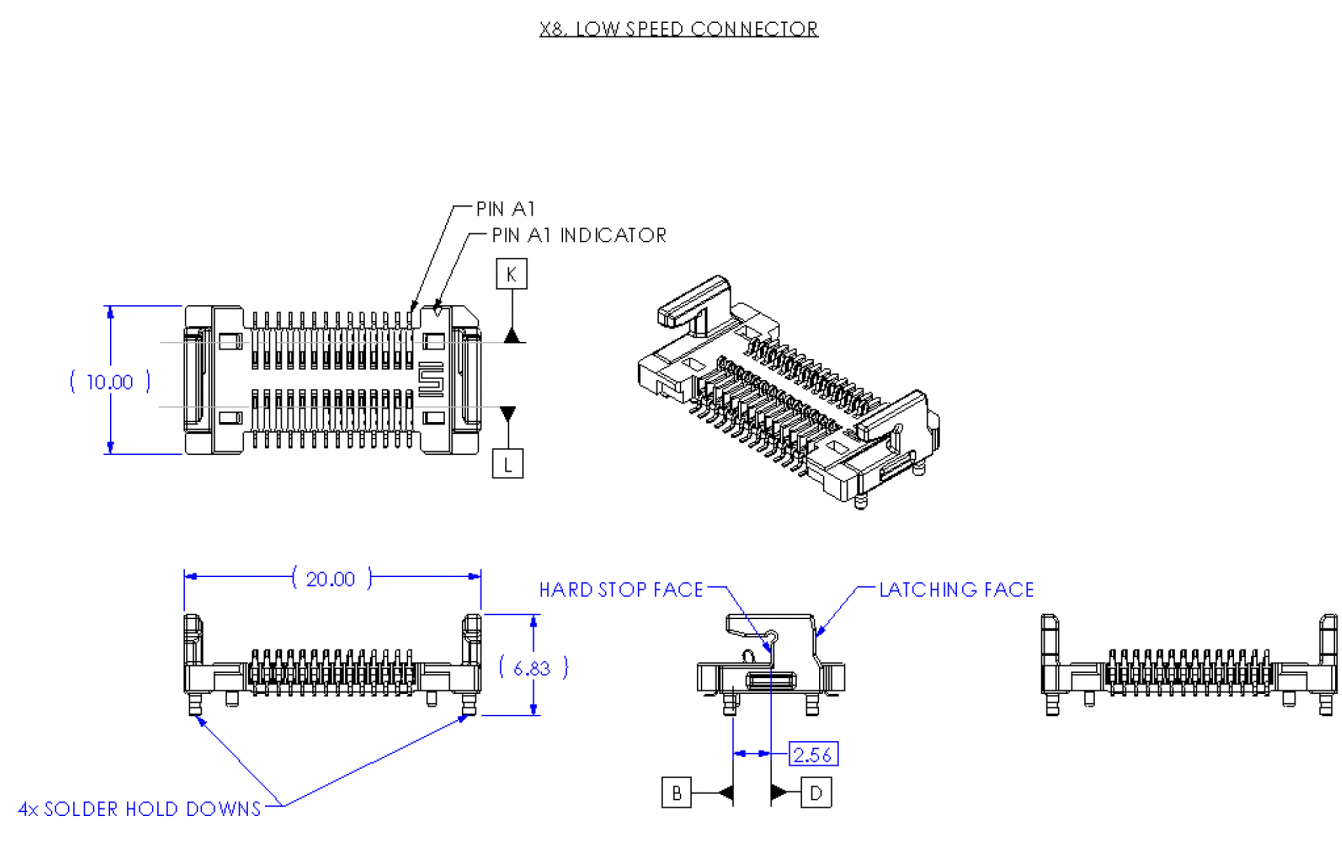


Figure 4-6: 8-Lane Low-Speed and Power Connector (28 position)

4.2.1.3 ×8 High-speed connector

The ×8 high-speed connector is a right-angle card-edge 50-position connector. This connector accepts a .062” (1.57mm) thick OBO PCB and has a 0.6mm contact pitch. The connector is applied with standard high-volume pick-and-place equipment. The high-speed and ground contacts are attached via conventional SMT reflow soldering while the metal connector shell simultaneously attaches to the host PCB using paste-in-hole soldering techniques.

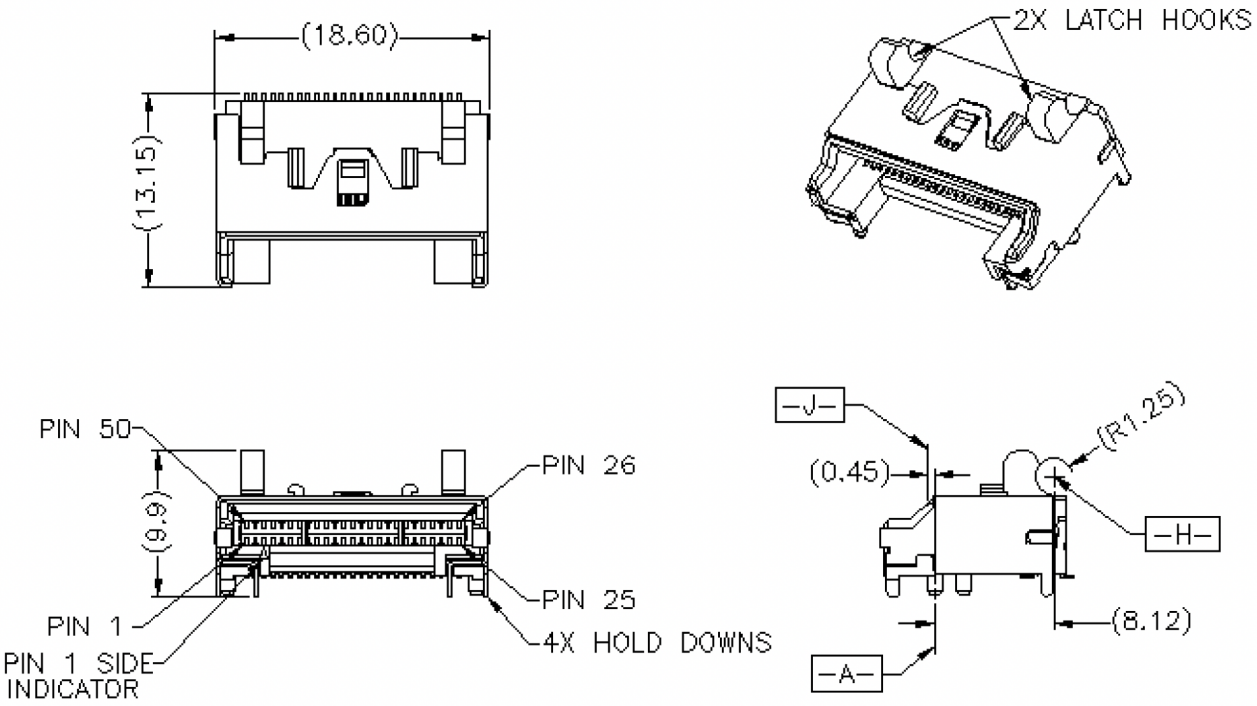
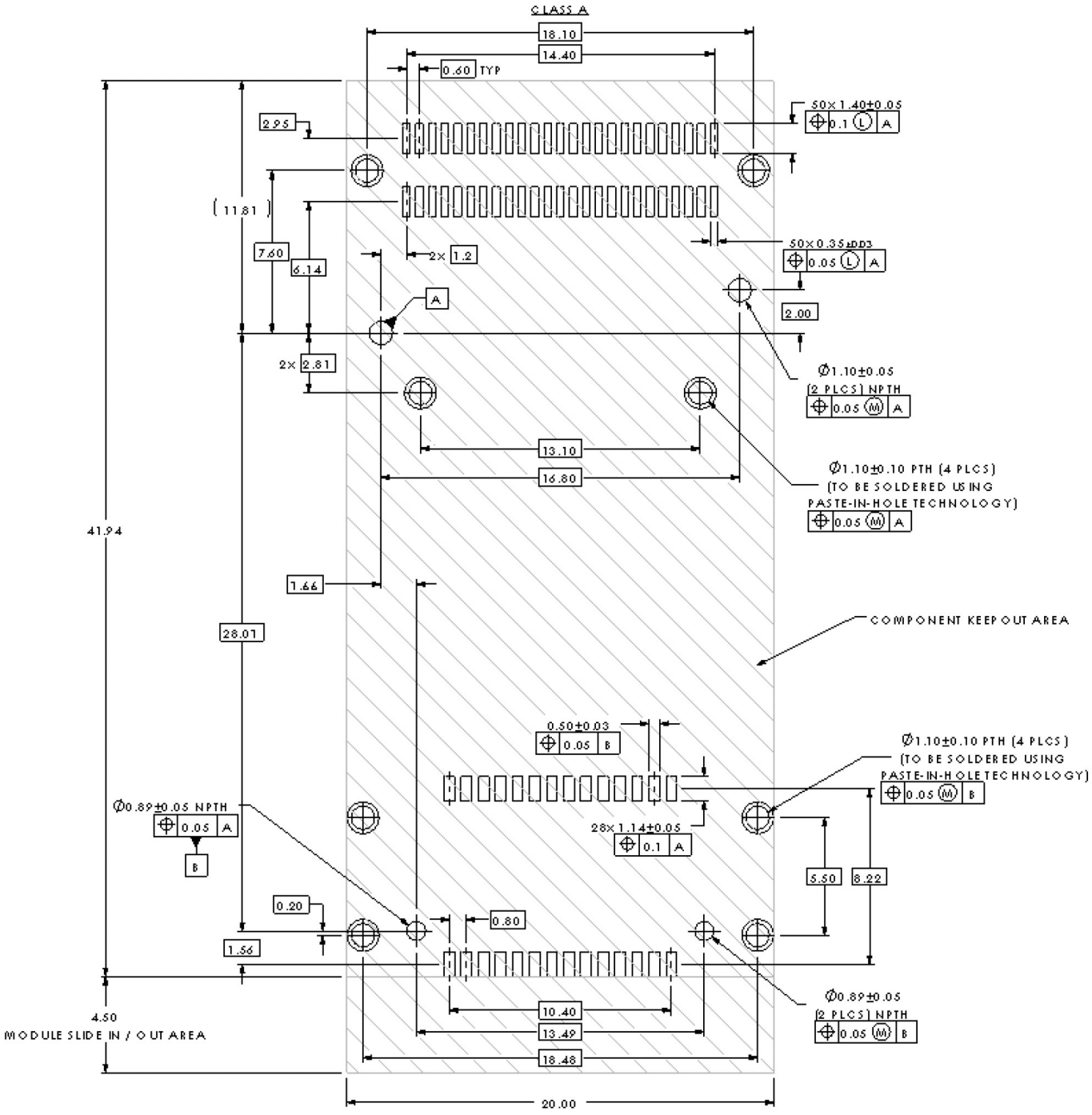


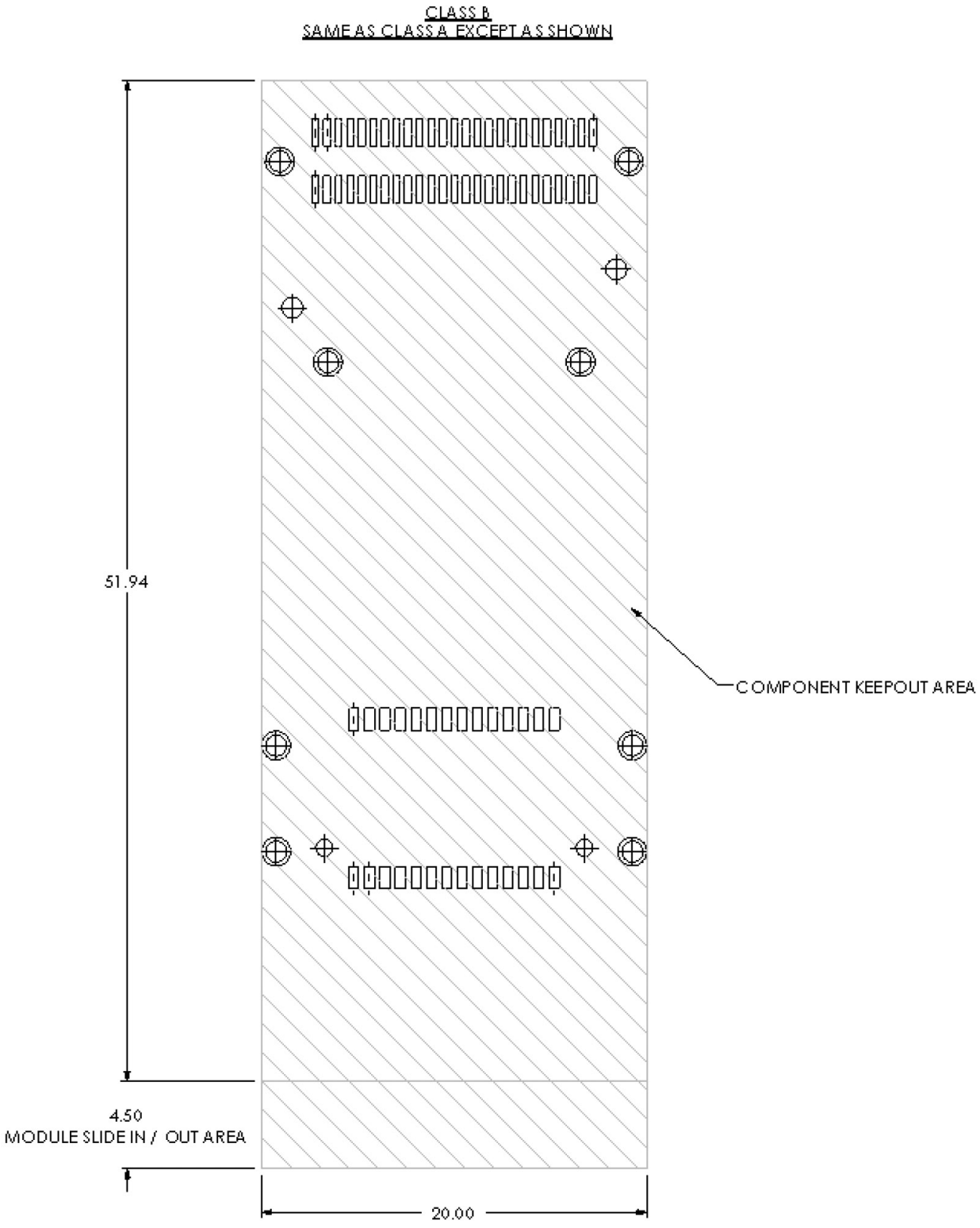
Figure 4-6: 8-Lane OBO High-Speed (50 Position)

4.2.1.4 ×8 Host Board

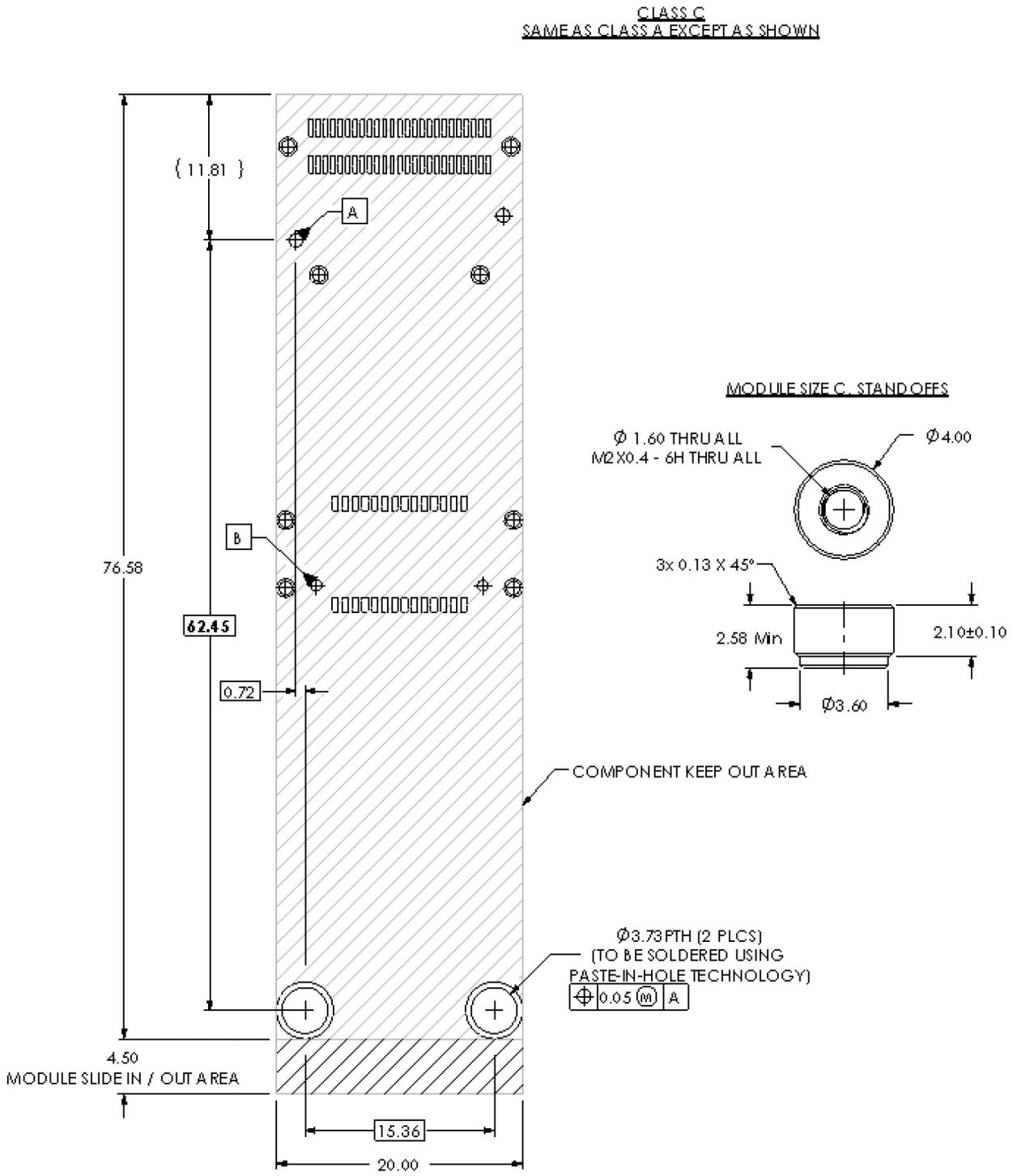
This section illustrates the host footprint that will support a full-pinout-capable 8-Lane OBO with both high-speed and low-speed contact zones. Note that the Class C host footprint includes a provision for two additional mounting features. The keep-out region is for components only, it is ok to have traces in that region.



Class A



Class B



Class C

Figure 4-8: Host Board Footprint Supporting Full Pinout as Defined by COBO for 8-Lane Applications

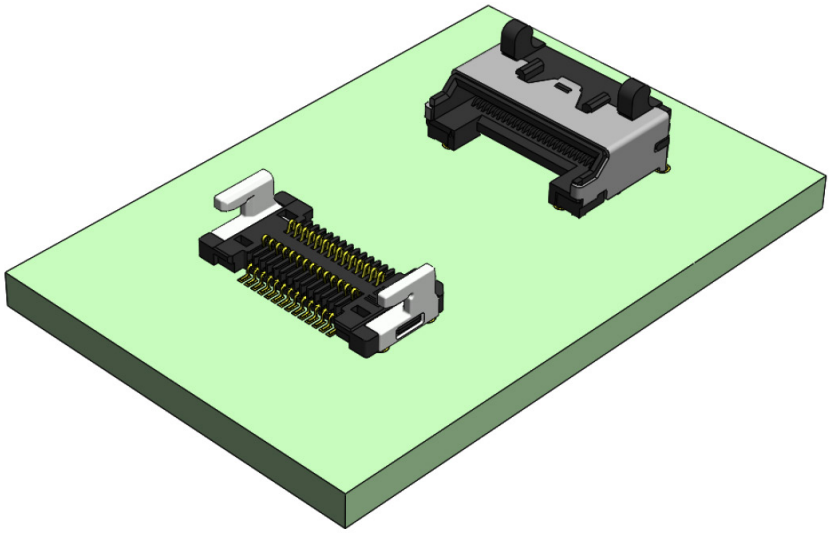


Figure 4-9: 8-Isometric View of x8 Connector Solution Set on the Host PCB

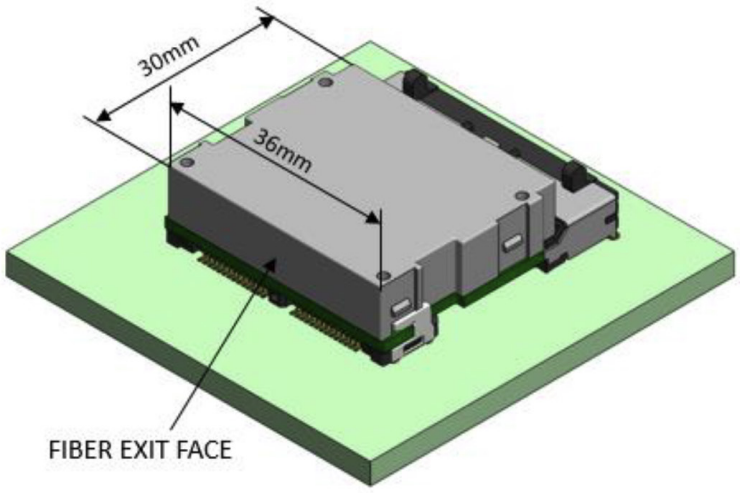
4.2.2 ×16 Solution

This section provides mechanical details of the ×16 OBO (400G) interconnect solution; the three ×16 OBO form factors (classes A, B, and C), host footprints, and mating application between the host connectors and the OBO. The ×16 form factors all utilize a two-electrical-connector solution for mounting to the host PCB. The electrical connectors used for all three OBO sizes are common to all three applications. The ×16 OBO is sized so that at least 16 OBOs can be fit into a 1RU equipment form factor. The OBO definition includes features to enable heat sink attachment to the OBOs by at least two methods.

4.2.2.1 ×16 OBO

The ×16 OBO is specified in 3 sizes, classes A, B, and C to enable use with multiple optical technologies and optical reach specifications. The primary difference between the three form factors is OBO length. See Figure 4-10.

Class A



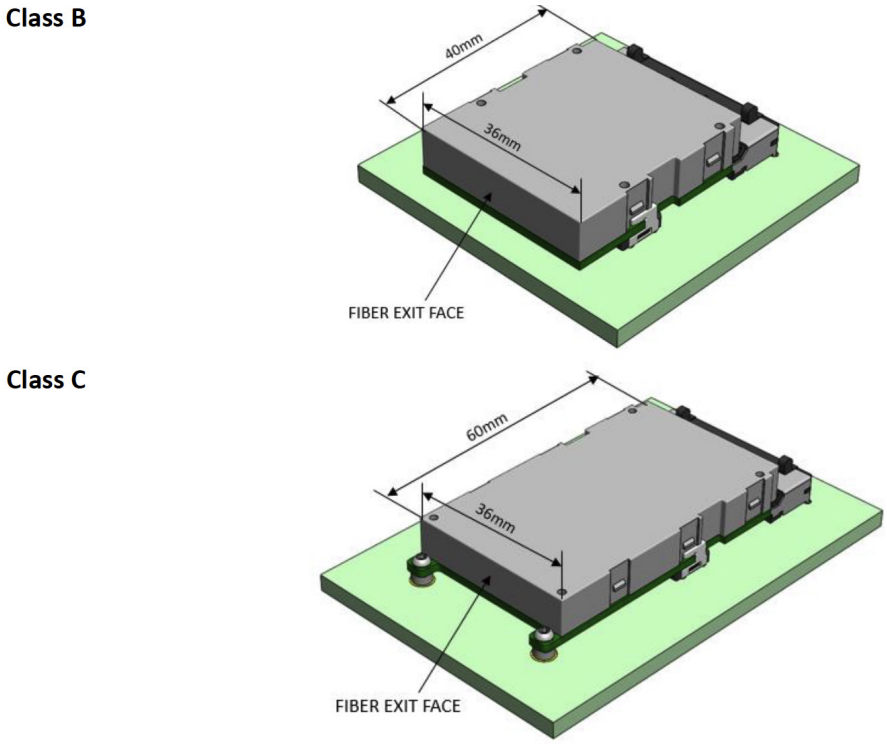


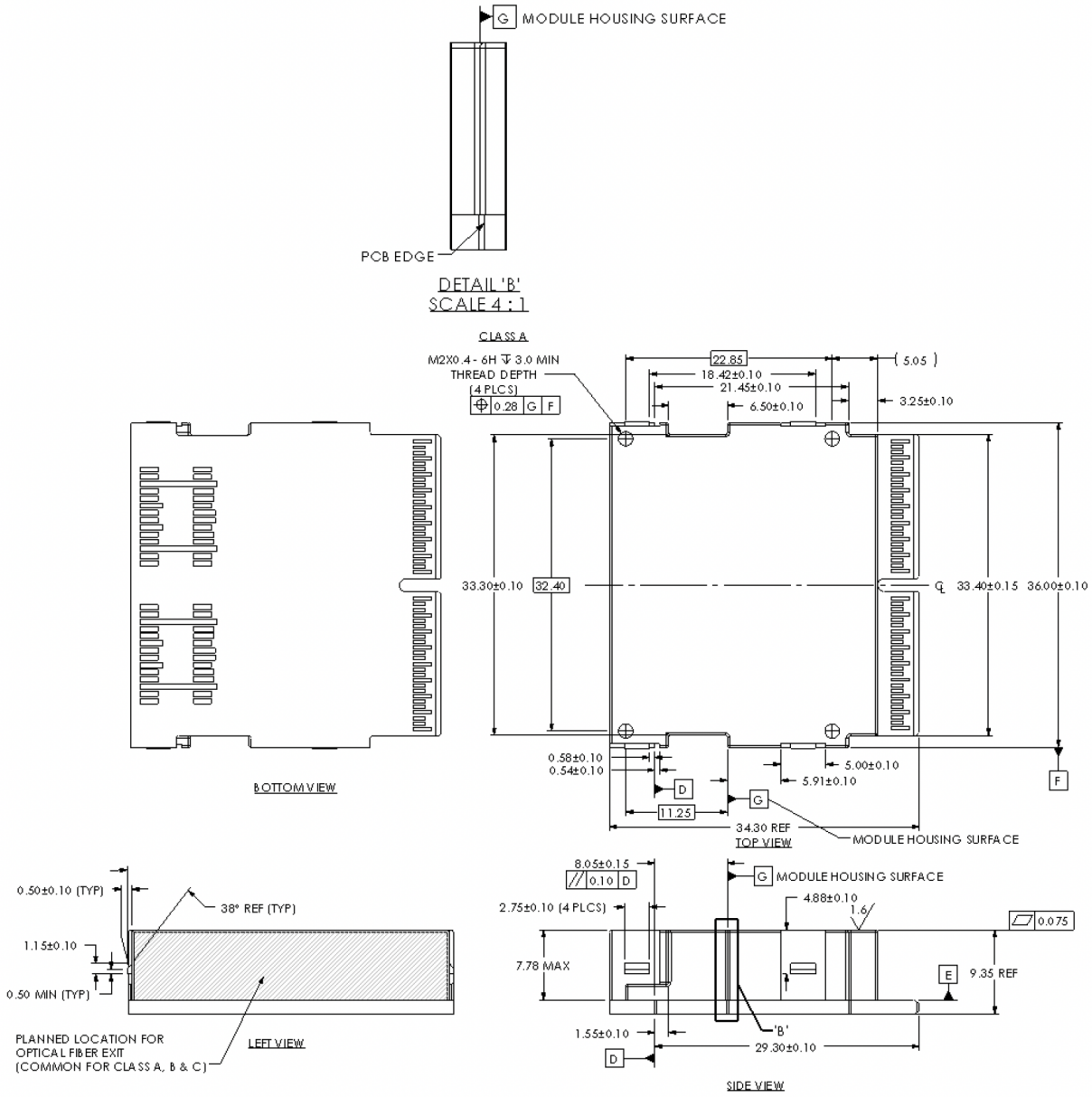
Figure 4-10: 8-16-Lane OBO Class A, B and C OBOs

The three OBO form factors, classes A, B, and C-are shown in the drawings below. The OBOs include threaded holes on the top surface for heat sink attachment, as well as latch features on the OBO sides for attaching heat sinks by a set of spring clips. These will be discussed further in 4.2.5.

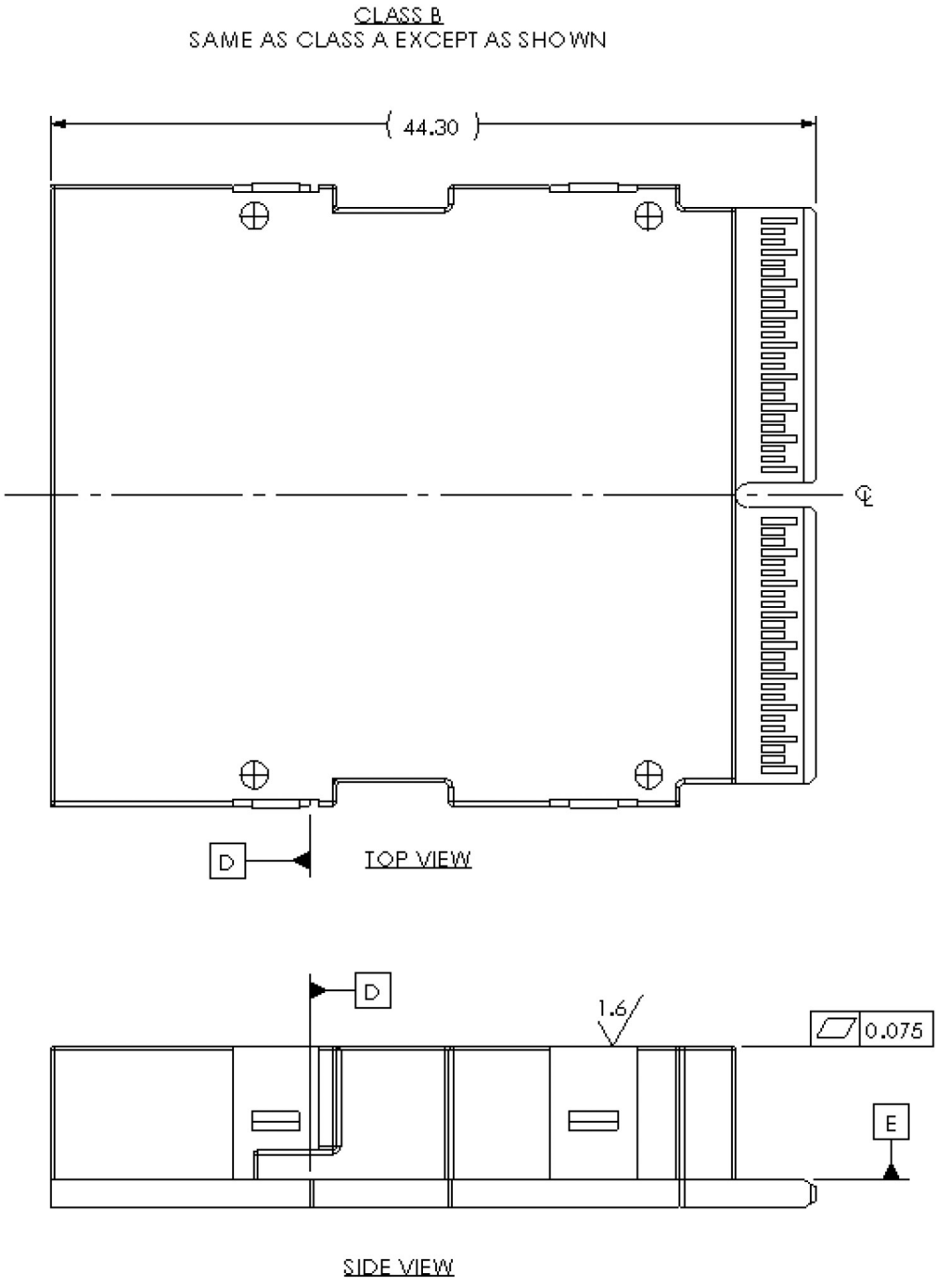
The datum structure used for the x16 OBO is identified in Table 4-2.

Datum	Description
A	Host board thru hole to accept high-speed connector guide post
B	Host board thru hole to accept low-speed connector guide post
D	Hard Stop on Low-Speed Connector
E	Bottom Surface of OBO Housing
F	Centerline of Width of OBO
G	OBO Reference Surface for Latch to Low-Speed Connector
H	OBO Reference Surface for Latch to High-Speed Connector
J	High-Speed Connector Mating Interface with OBO PCB Pads
K	Low-Speed Connector Mating Interface with Row 1 OBO PCB Pads
L	Low-Speed Connector Mating Interface with Row 2 OBO PCB Pads
M	Centerline of Width of OBO PCB
N	Top Surface of OBO PCB

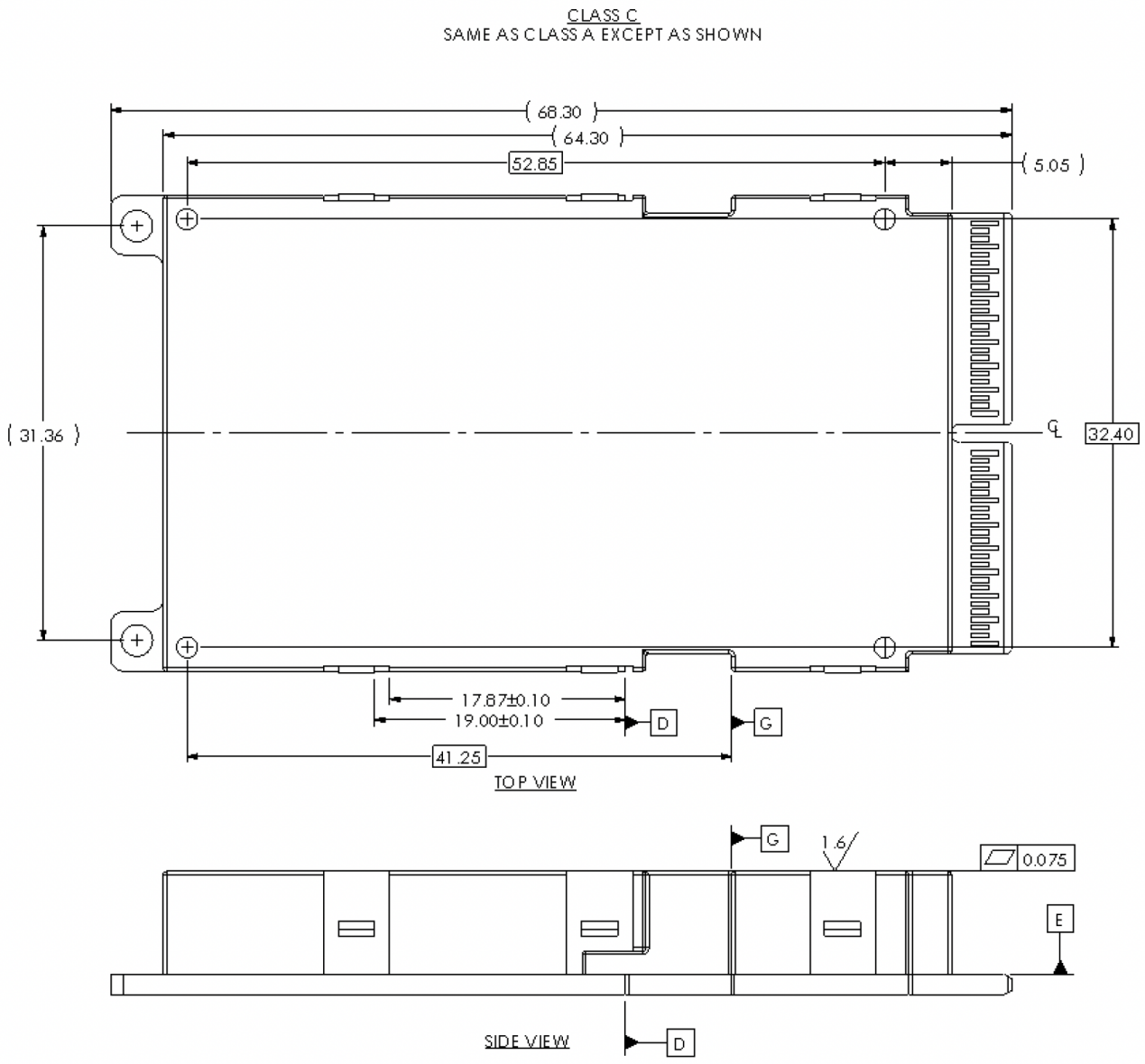
Table 4-2: Datum Structure Used for x16 OBO



Class A



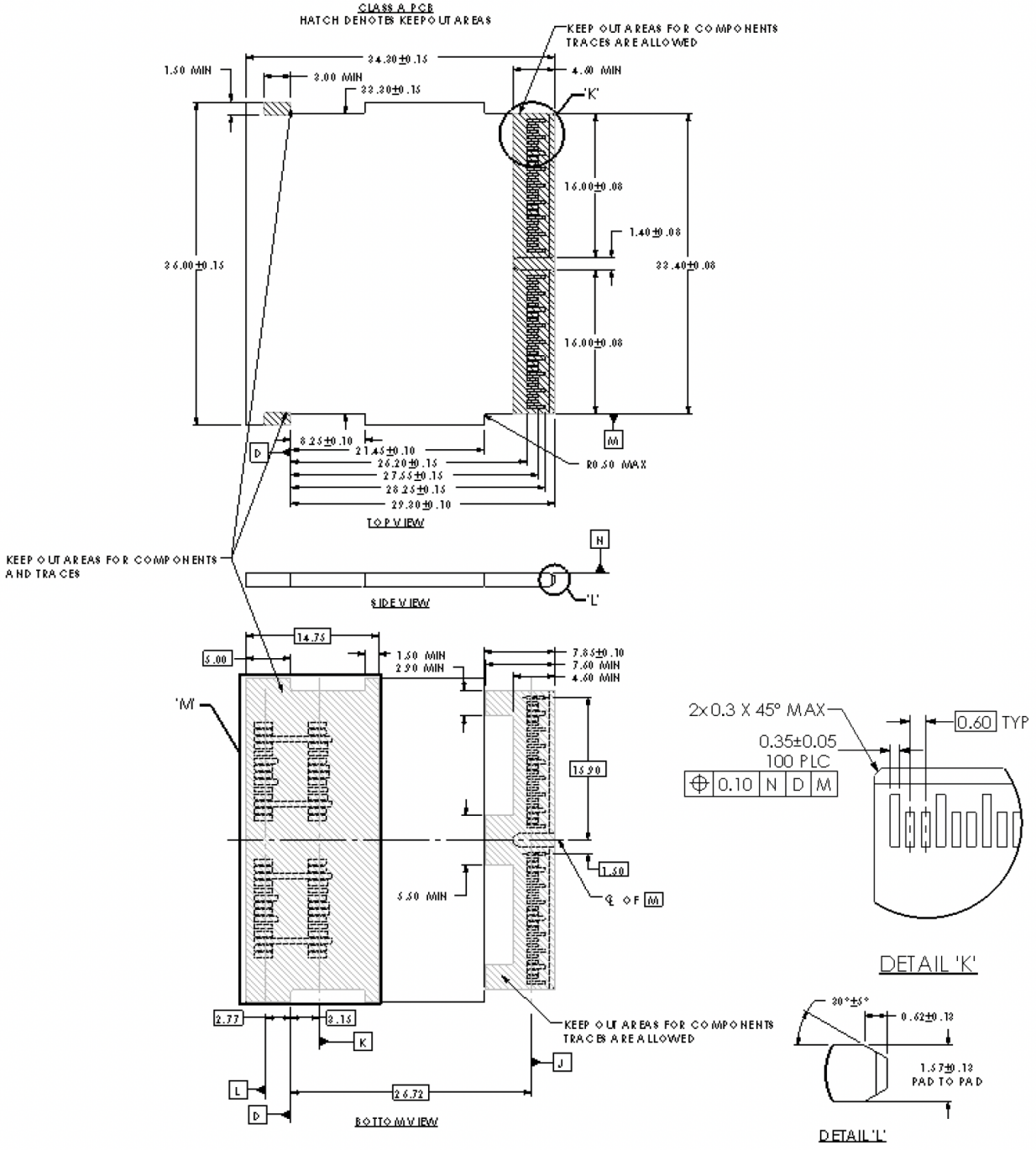
Class B



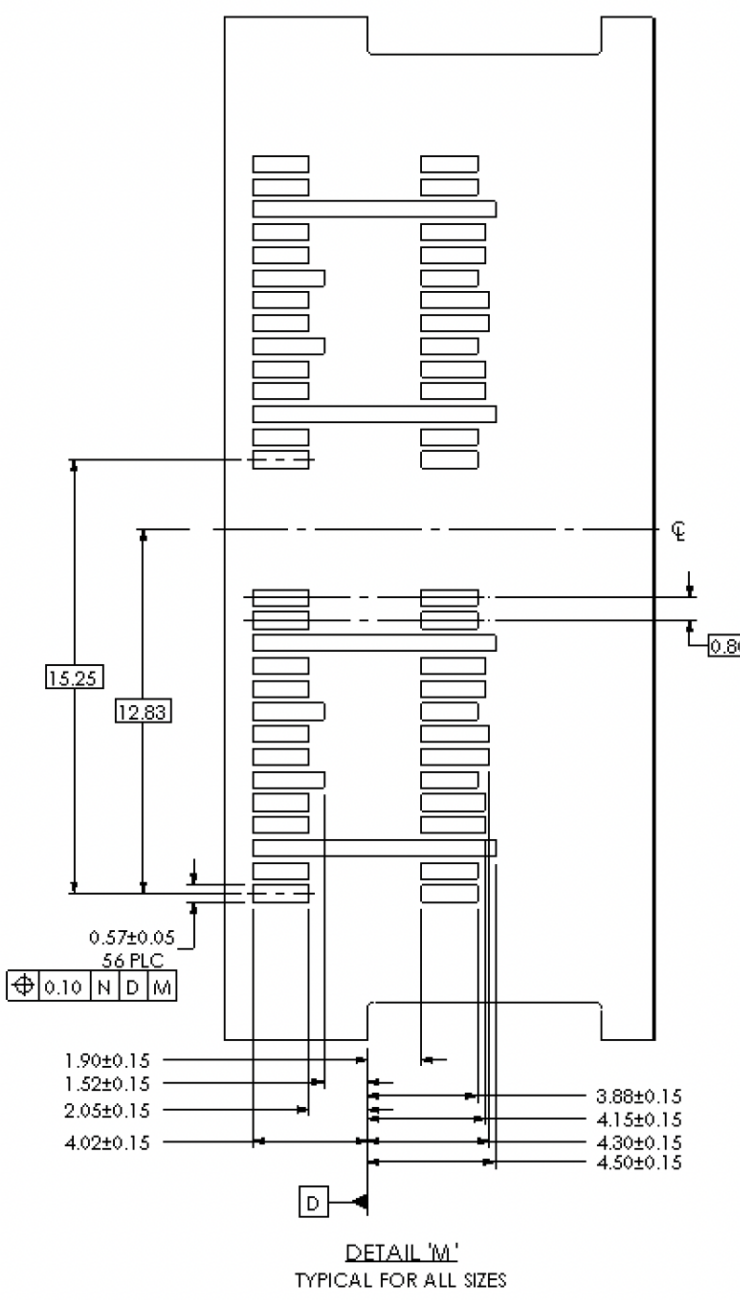
Class C

Figure 4-11: 16-Lane OBO Form Factors Class A, B and C

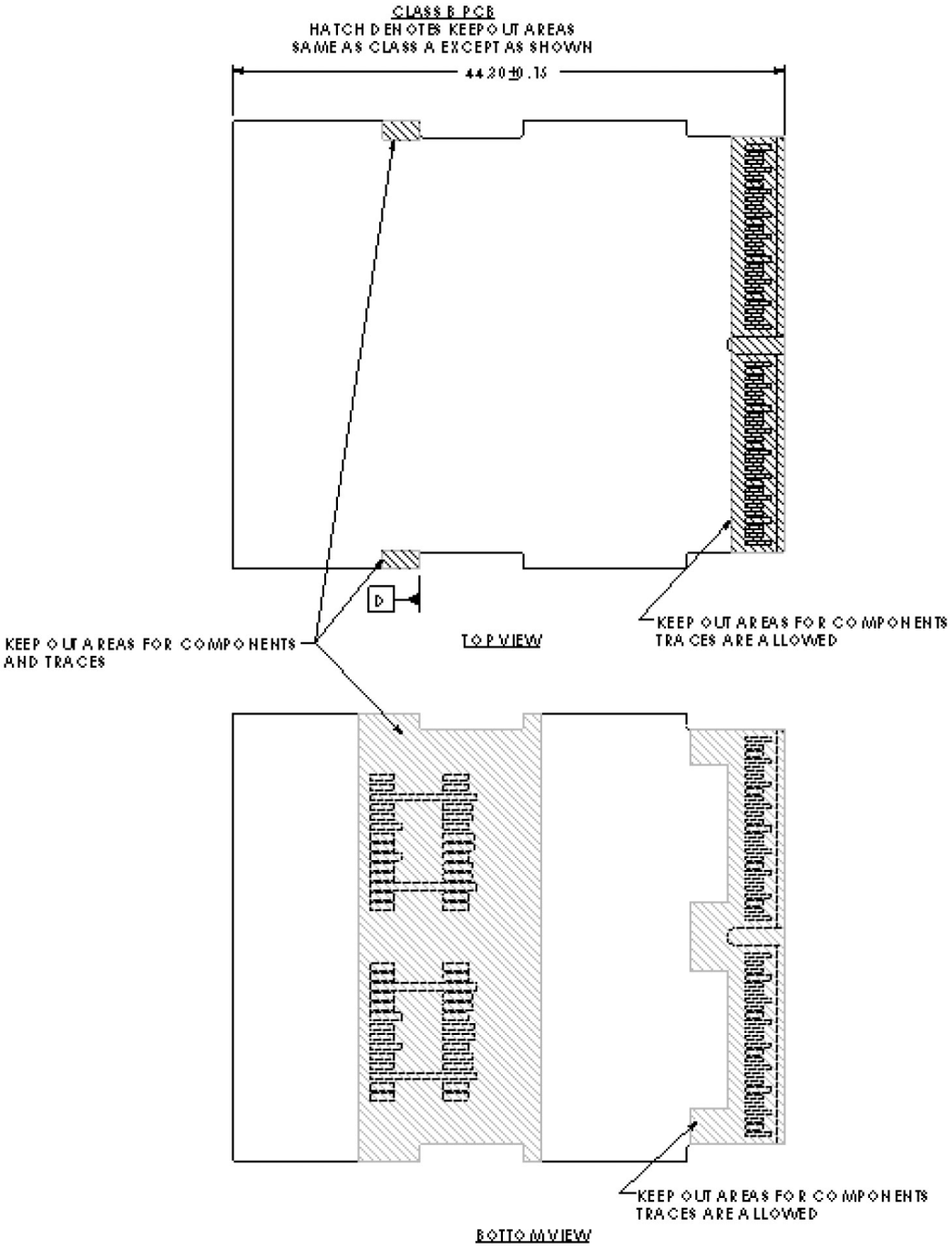
The OBO PCBs for the three form factors are shown in Figure 4-12.



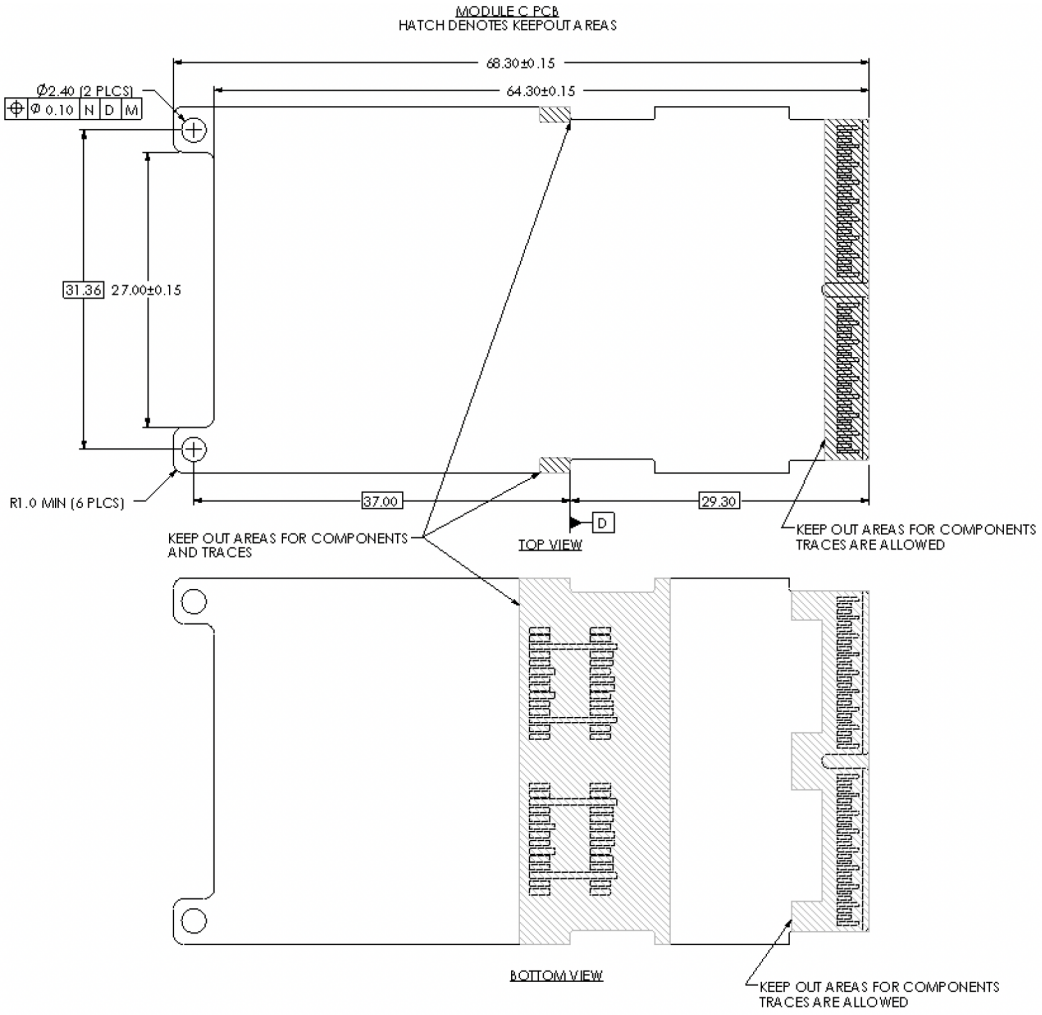
Class A



Class A, B, & C – Detail 'M'



Class B



Class C

Figure 4-12: 16-Lane OBO PCB, Class A, B and C

4.2.2.2 ×16 Low-speed Connector

The ×16 Low-speed connector is an integrated assembly comprised of 56 contact positions on 0.8mm contact pitch. The low-speed connector functions by making z-axis contact with metalized pads on the bottom side of the OBO PCBs. The connector includes two integrated metal “J hook” features that engage the OBO and maintain the necessary clamping force between the OBO and connector. The low-speed connector also serves as the hard stop surface when the OBO is mating to the high-speed and low-speed connectors to prevent over insertion. The connector is applied with standard high-volume pick-and-place equipment. The power and signal contacts are attached via conventional SMT reflow soldering and the integrated hook features simultaneously attach to the host PCB using paste-in-hole soldering techniques.

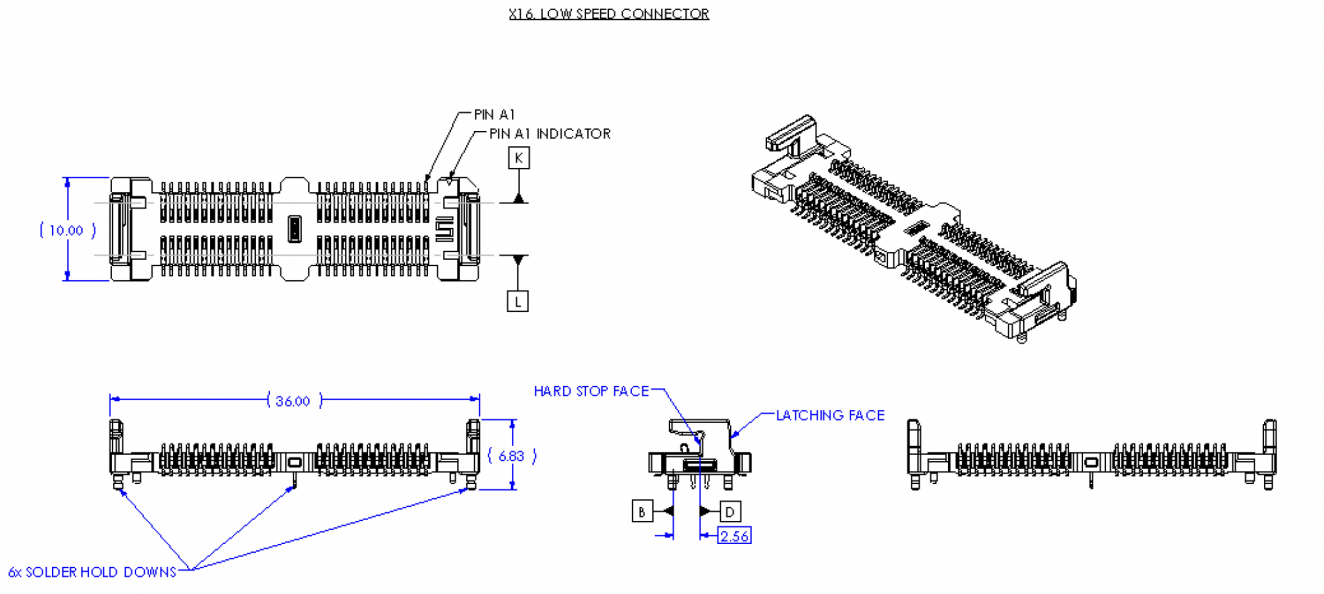


Figure 4-13: 16-Lane OBO Low-Speed and Power Connector (56 Position)

4.2.2.3 ×16 High-Speed Connector

The ×16 high-speed connector is a right-angle card-edge 100-position connector. This connector accepts a .062" (1.57mm) thick OBO PCB has a 0.6mm contact pitch. The 100 position high-speed connector is divided into two sections, each with 50 contact positions. The connector is applied with standard high-volume pick-and-place equipment. The high-speed and ground contacts are attached via conventional SMT reflow soldering while the metal connector shell simultaneously attaches to the host PCB using paste-in-hole soldering techniques.

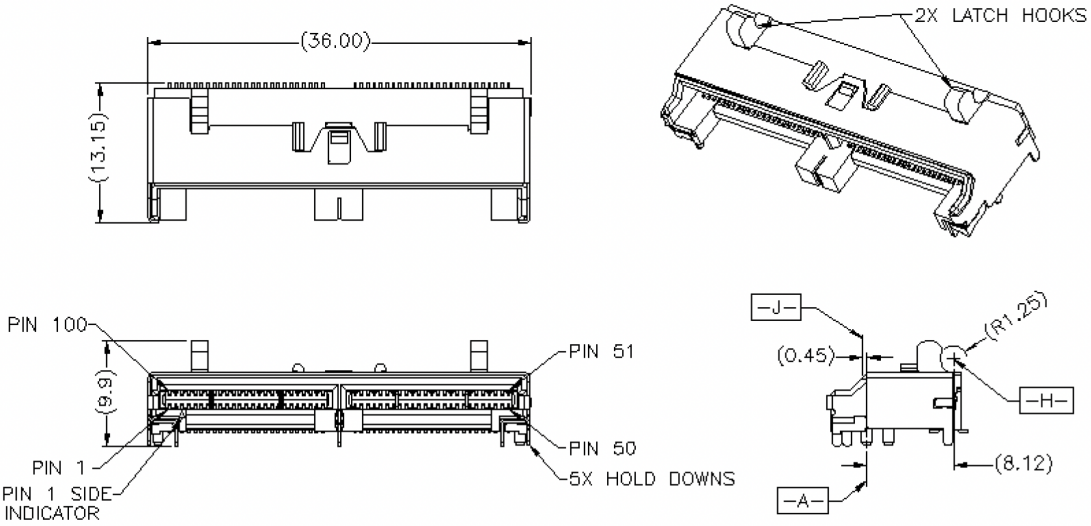
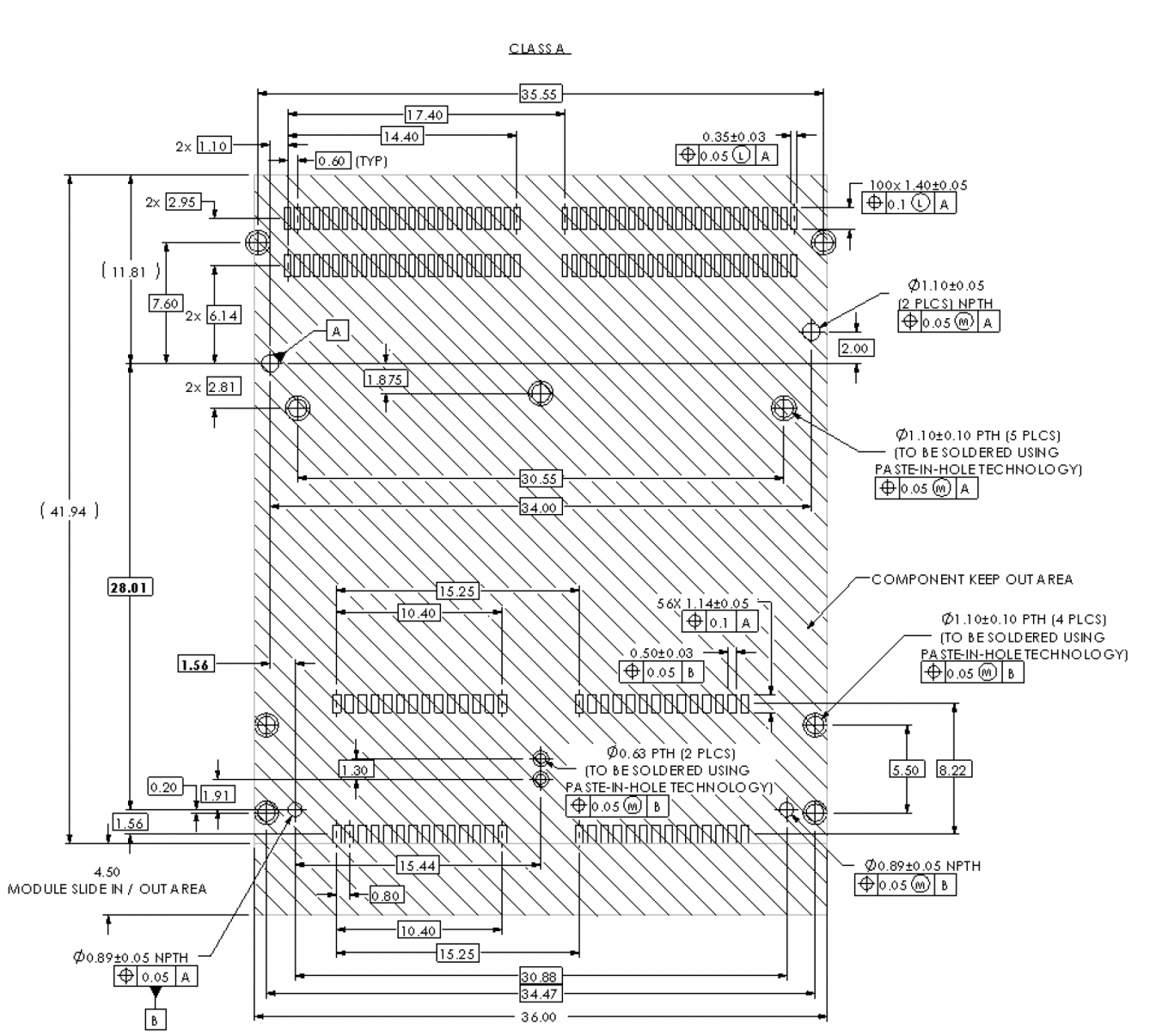


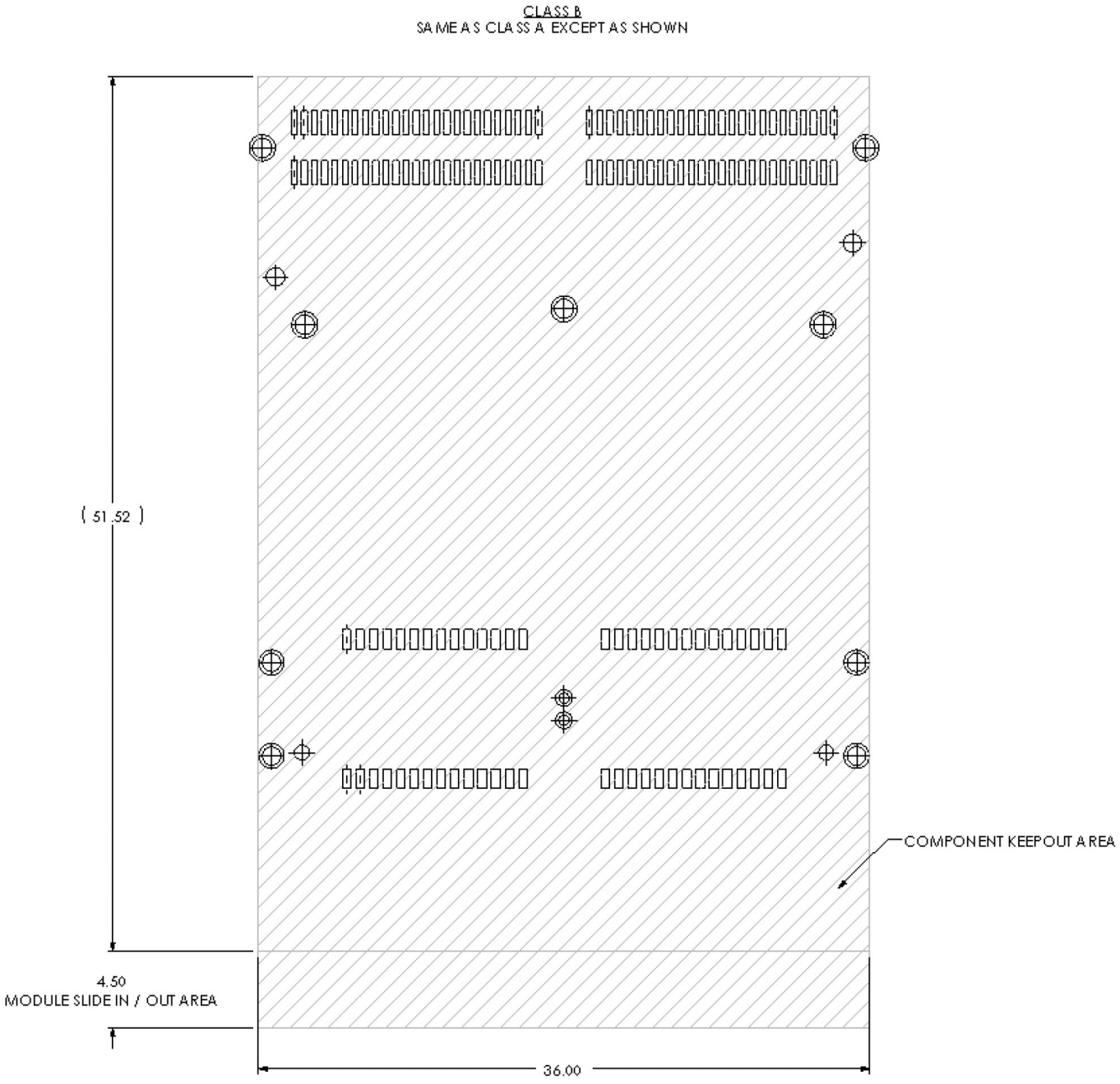
Figure 4-14: 16-Lane OBO High-Speed Connector (100 Position)

4.2.2.4 ×16 Host Board

This section illustrates the host footprint that will support a full-pinout-capable 16-Lane OBO with both high-speed and low-speed contact zones. Note that the Class C host footprint includes a provision for two additional mounting features. The keep-out region is for components only, it is permissible to have traces in that region.



Class A



Class B

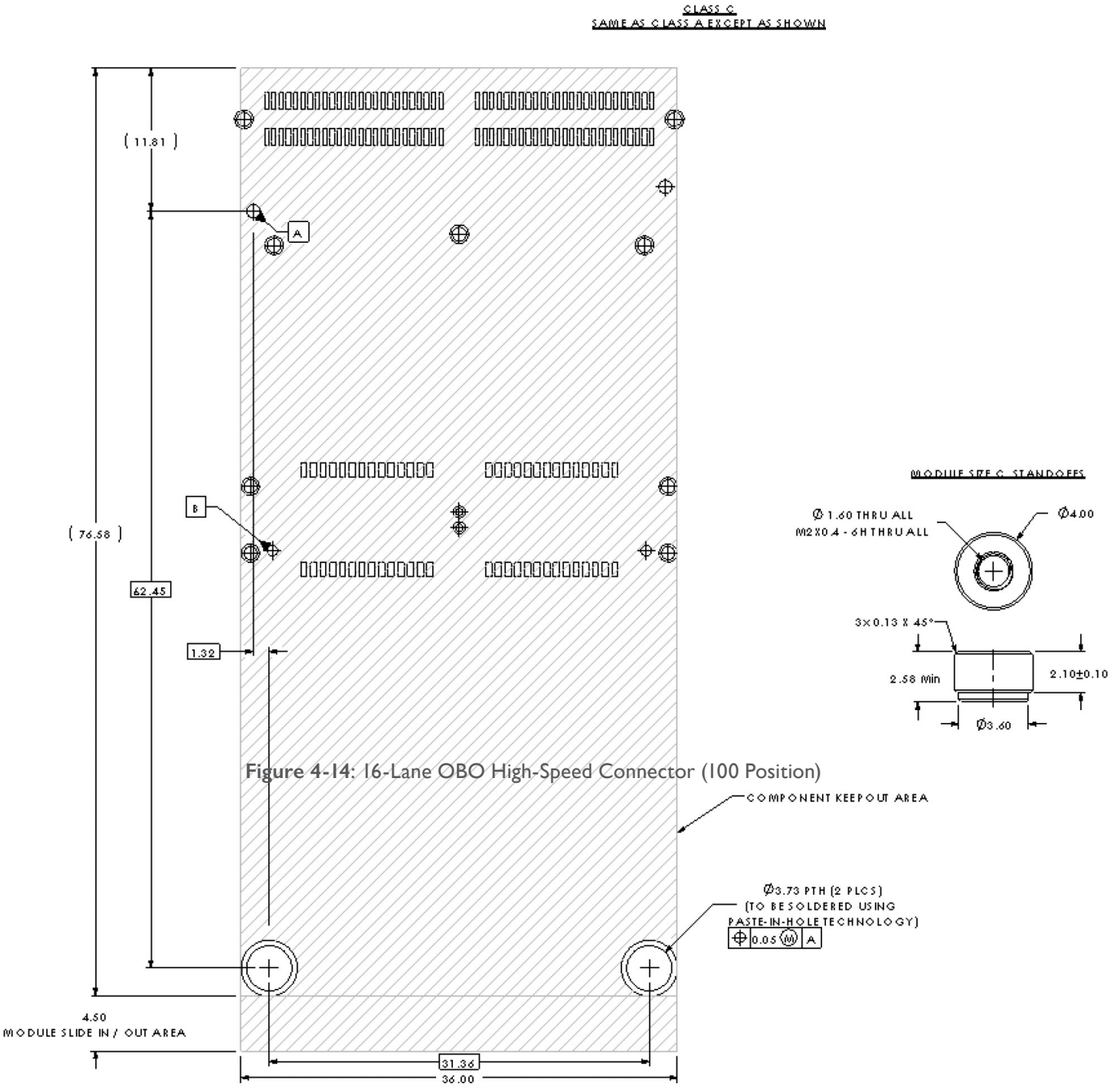


Figure 4-14: 16-Lane OBO High-Speed Connector (100 Position)

Class C

Figure 4-15: Host Board Footprints Supporting Full Pinout as Defined by COBO for 16-Lane Application

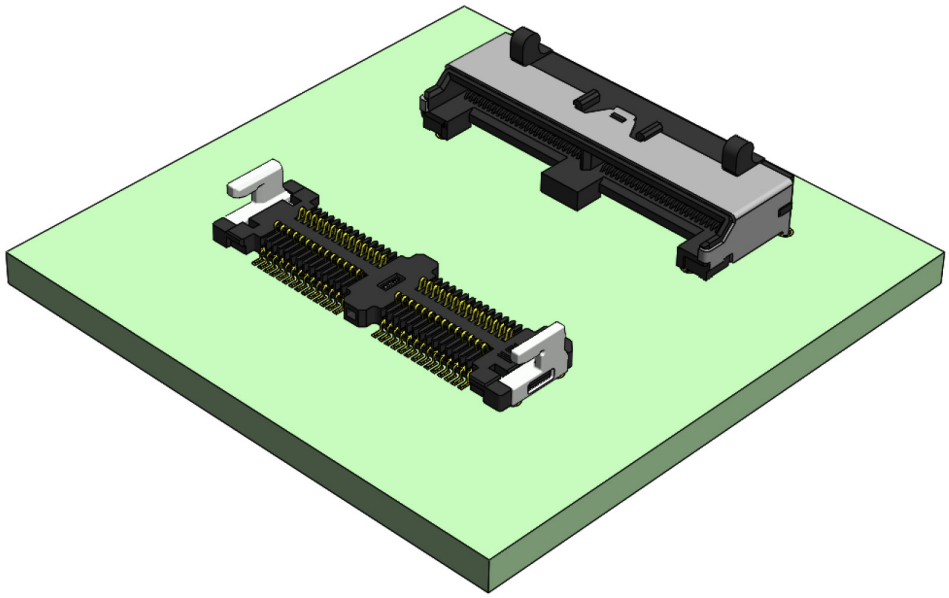


Figure 4-16: Isometric View of x16 Connector Solution Set on the Host PCB

4.2.3 OBO Latching to Host Connectors – common to both ×8 and ×16 solutions

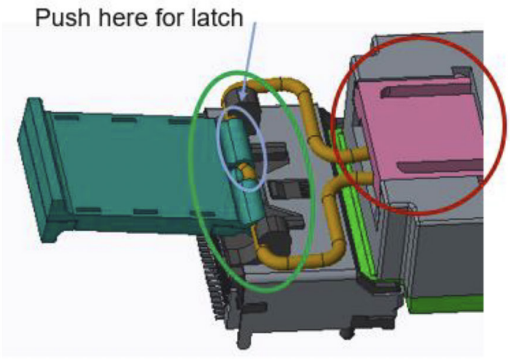
Both the low-speed and high-speed connectors have pre-mating features to ensure the OBO is correctly aligned prior to the entry of the card edge into the receptacle, minimizing the possibility of misalignment damage to either part. These protection features are integrated into the connector and OBO. Since the pre-alignment features work together as a system with the latching please refer to Section 4.2.3.1 and 4.2.3.2 for latching information.

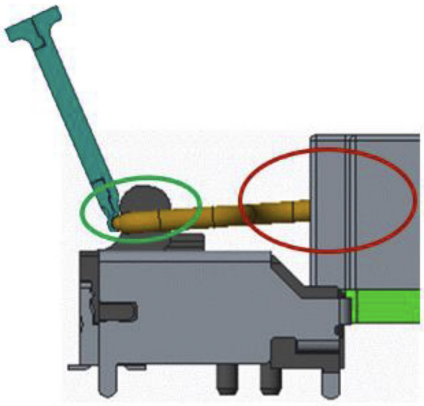
Latching to either the low-speed or the high-speed connector must be supported by the OBO. Latching to both connectors is not recommended.

4.2.3.1 Latching to the High-speed Connector

The system for latching to the high-speed connector is a simple, low-cost latch system that has been previously tested and proven. The key elements are a molded hook on the high-speed connector and a spring/latch arm on the OBO housing. The latch arm assembly is a simple metal or plastic piece which has a spring function to provide a secure, robust mechanism that ensures the OBO is always fully seated to the high-speed connector to obtain the best possible signal-integrity performance. This high-speed connector latch minimizes impedance discontinuities between the connector and the OBO card edge caused by mating tolerance accumulation. Impedance discontinuities are especially critical with PAM4 signals at 56Gbps and future applications at 112Gbps PAM4. Another key benefit of the high-speed-connector latch system is the reliability and robustness provided by the constant spring tension between the OBO and both the connectors over all environmental conditions and stresses. The latch arm pulls the OBO into both the high-speed receptacle cavity and the low-speed-connector J hooks. In Figure 4-17, the latch hook on the high-speed connector and the latch arm protruding from the OBO (green circles) are normative aspects of the high-speed connector latch. The integration implementation of the latch arm into the OBO and its associated spring function as shown in Figure 4-17 (red circles) represent an example implementation and is provided purely as an informative method. The keep out zone shown on the OBO is sized according to the shown example latch arm attachment to the OBO and spring mechanism. A different implementation by an OBO maker will likely have a different-sized keep out zone. The intent of the keep out zone is to indicate the approximate area that may not be conducting thermal energy to the heat sink for the example implementation.

Latched

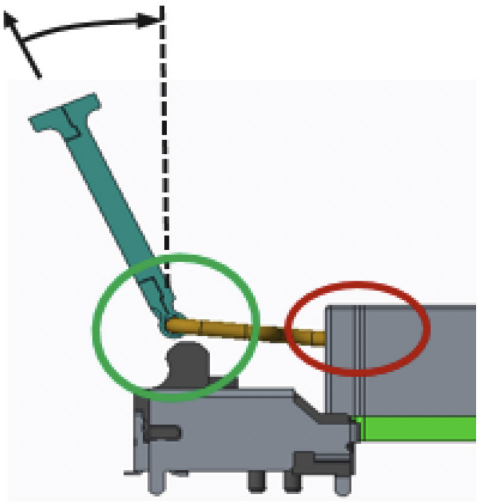




Informative aspects:

Normative aspects:

Unlatched



Informative aspects:

Normative aspects:

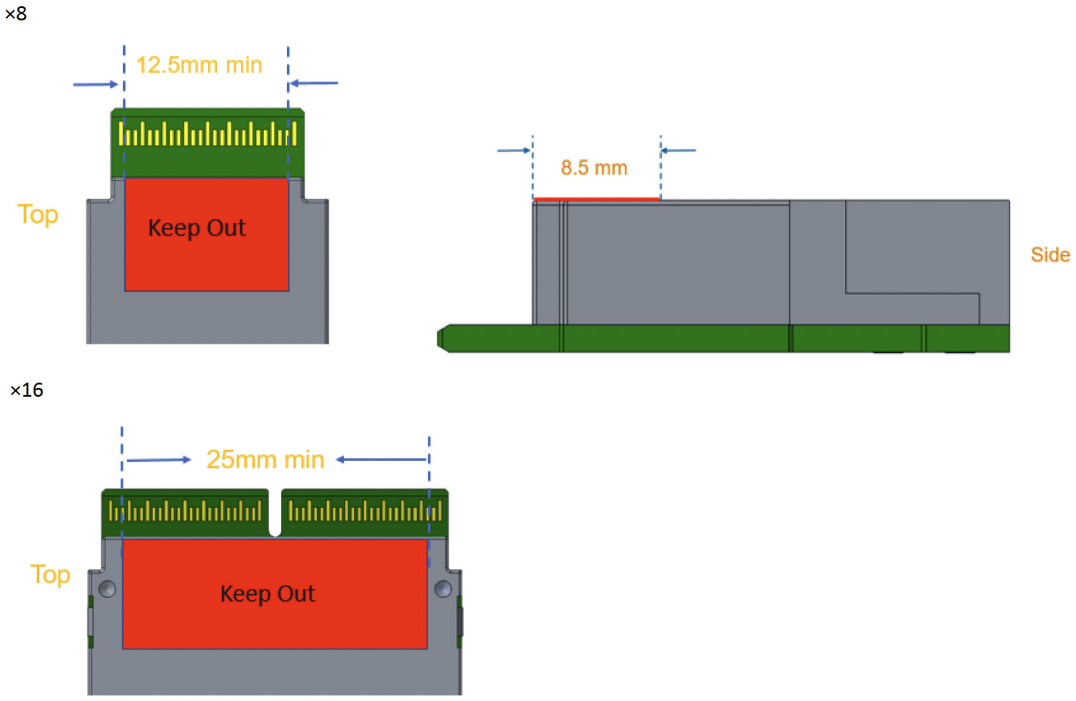


Figure 4-17: Latching to the High-Speed Connector and OBO Latch Keep Out Areas

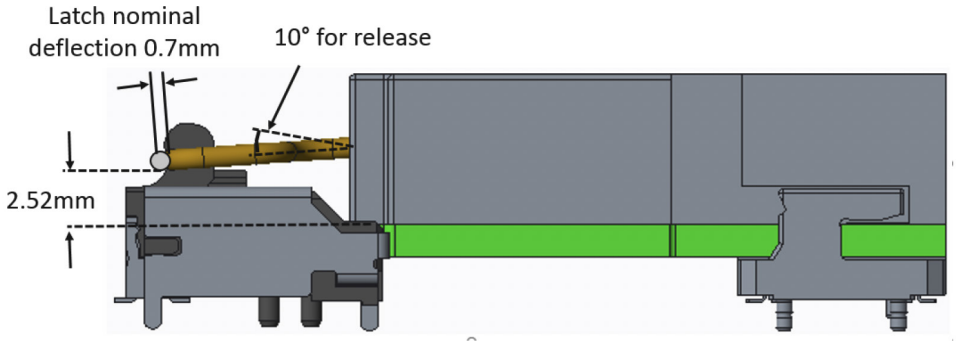
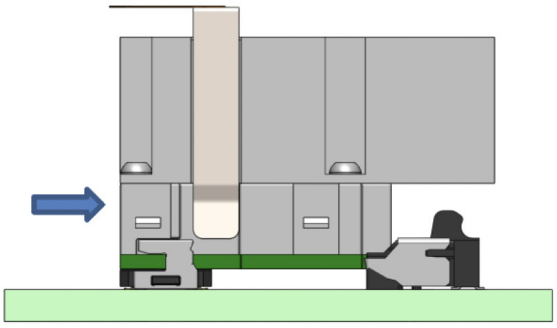


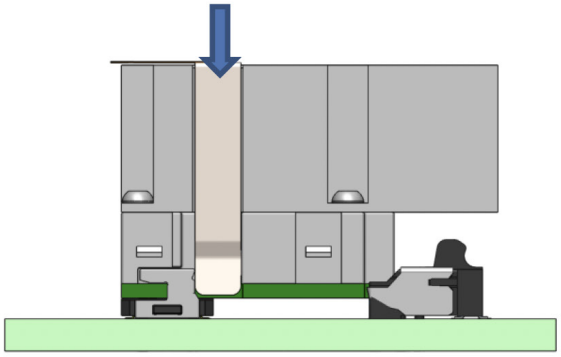
Figure 4-18: High-Speed OBO Latch Dimensions

4.2.3.2 Latching to the Low-Speed Connector

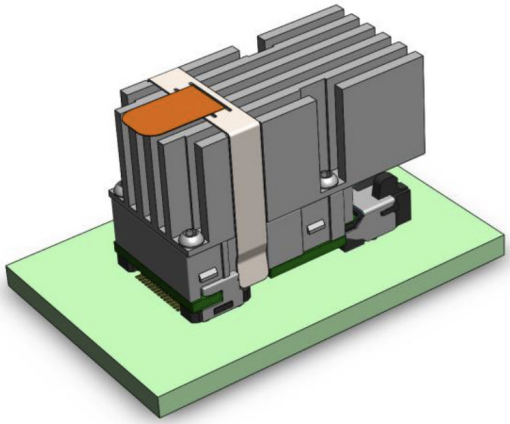
The latch system for the low-speed connector is based on a simple U-Clip latch piece (sheet metal) which is inserted in a channel in the side of the OBO. This U-Clip prevents the OBO from disengaging from the connectors by making contact with the back side of the low-speed-connector J hooks. This is a very-low-cost solution that does not provide the constant spring tension of the high-speed-connector latch explained in Section 4.2.3.1. The U-clip latch utilizes the unused volume of the OBO, and does not take up any of the OBO or heatsink interface area. It can work for heatsink fins oriented in any direction. See Figure 4-19.



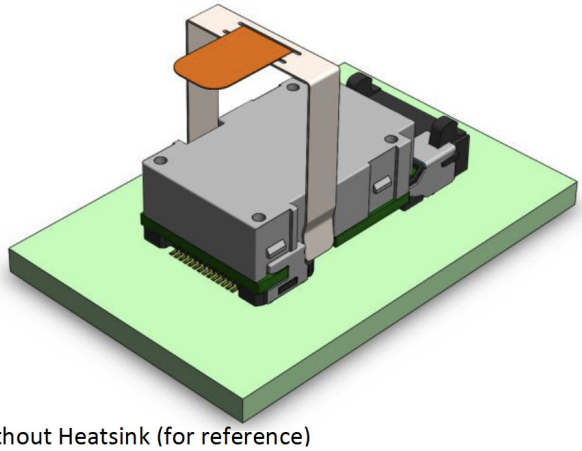
Insert Module with U-Clip up



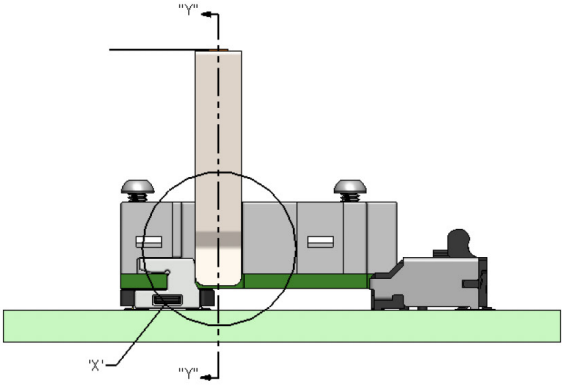
Press U-Clip down to Lock

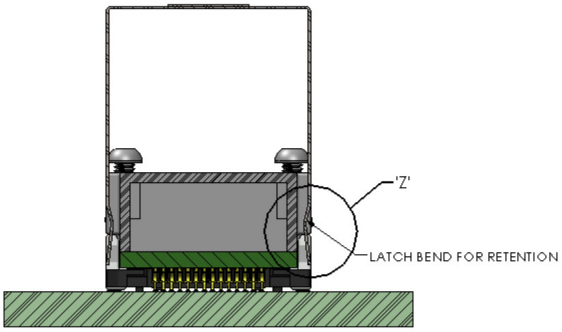


With Heatsink



Without Heatsink (for reference)





SECTION "Y"-"Y"
SCALE 2 : 1

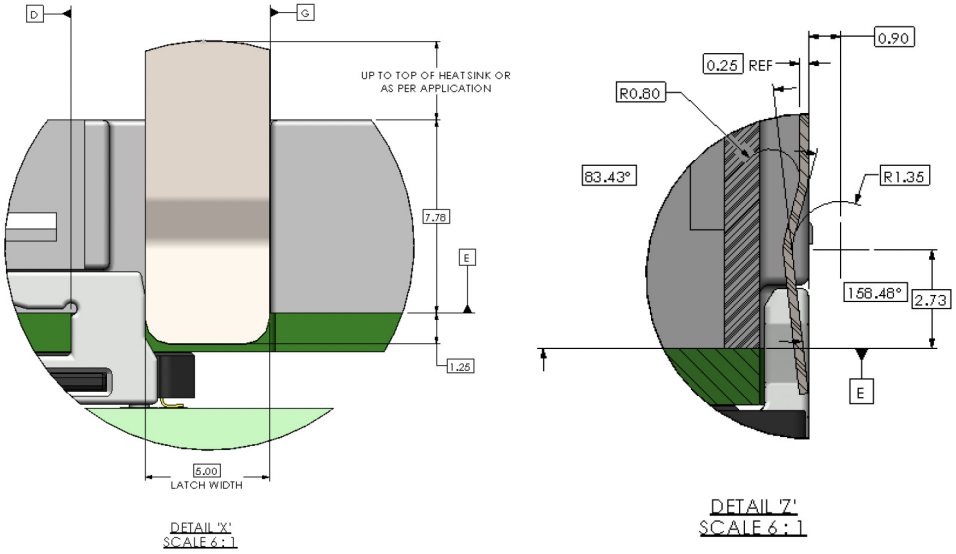


Figure 4-19: Latching to the Low-Speed Connector

4.2.4 OBO Insertion, Extraction and Retention Forces

Parameter	X8		X16		Units	Comments
	Min	Max	Min	Max		
Insertion Force		50		90	N	
Extraction Force		30		50	N	
OBO Retention in connector system	50		50		N	No damage to OBO below 50N with retention mechanism engaged
High-Speed Connector Retention to PCB	30		30		N	Force to be applied perpendicular to host. No damage to connector or host PCB below 30N
Low-Speed Connector Retention to PCB	30		30		N	Force to be applied perpendicular to host. No damage to connector or host PCB below 30N
Insertion/Removal Cycles-OBO	50		50		Cycles	Number of cycles for an individual OBO
Insertion /Removal Cycles-Connector	50		50		Cycles	Number of cycles for the connectors

Table 4-3: OBO Insertion, Extraction and Retention Forces

4.2.5 Heat Sink Attachment

Managing the OBO case temperature due to the power dissipated in the OBO is critical to optics reliability and system-level thermal management. The OBO must support one of the two following options for heat-sink attachment to the OBO.

4.2.5.1 Screwed Heat Sink Attachment Option

This attachment method uses the M2-threaded holes on the top of the OBO to clamp down a heat sink, with thermal interface material between the two parts. These holes can be used to screw a heat sink and thermal interface material to the OBO. The advantage of the screws is the additional pressure that can be applied to the OBO-heat sink interface.
See Figure 4-20.

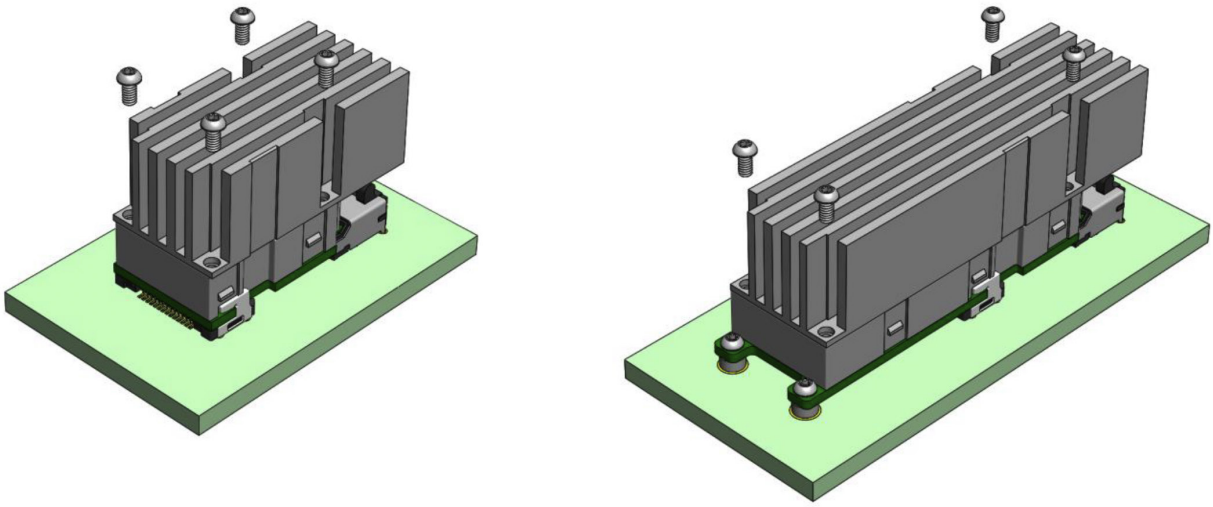
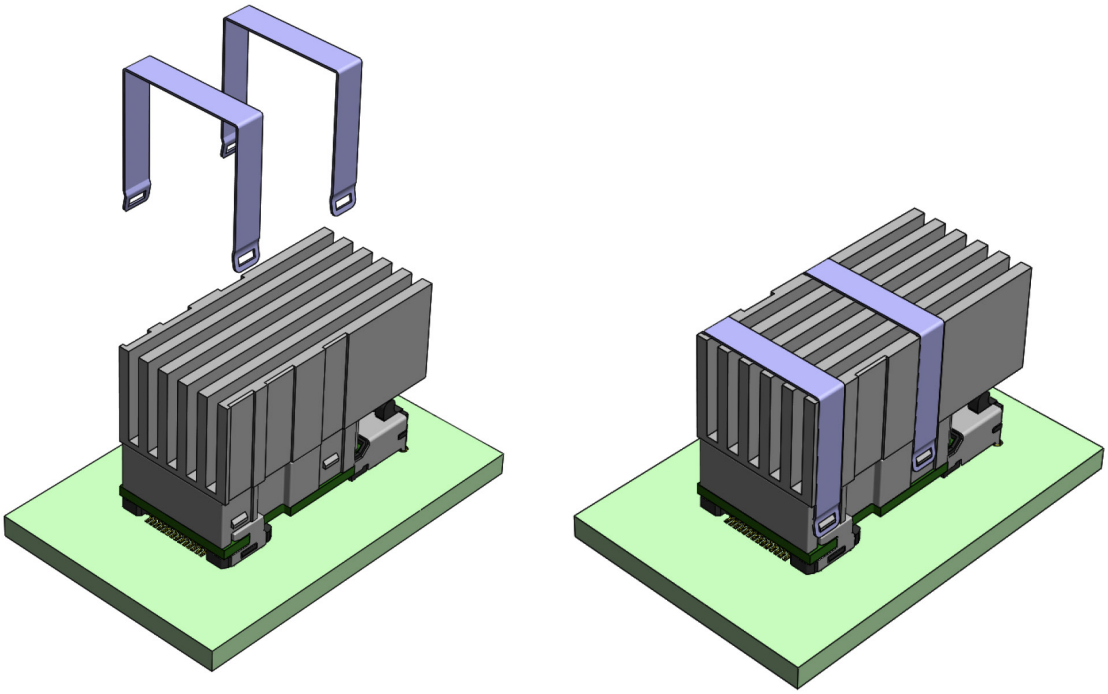


Figure 4-20: Heat Sink Attachment by M2 Screw

4.2.5.2 Clip Based Heat-Sink Attachment Option

An alternate solution is to attach the heat sink to the OBO with heat sink clips similar to those used on the cages for traditional pluggable modules. An important improvement is that a thermal interface material can also be used. The OBO has latch features on the side of the OBO which receive the spring clip. An important consideration of this type of thermal management is the pressure generated between the OBO and heat sink by the spring clip design. It is important to design the clip for maximum spring force and to ensure there is adequate working range for the clip to generate and maintain those forces. See Figure 4-21.



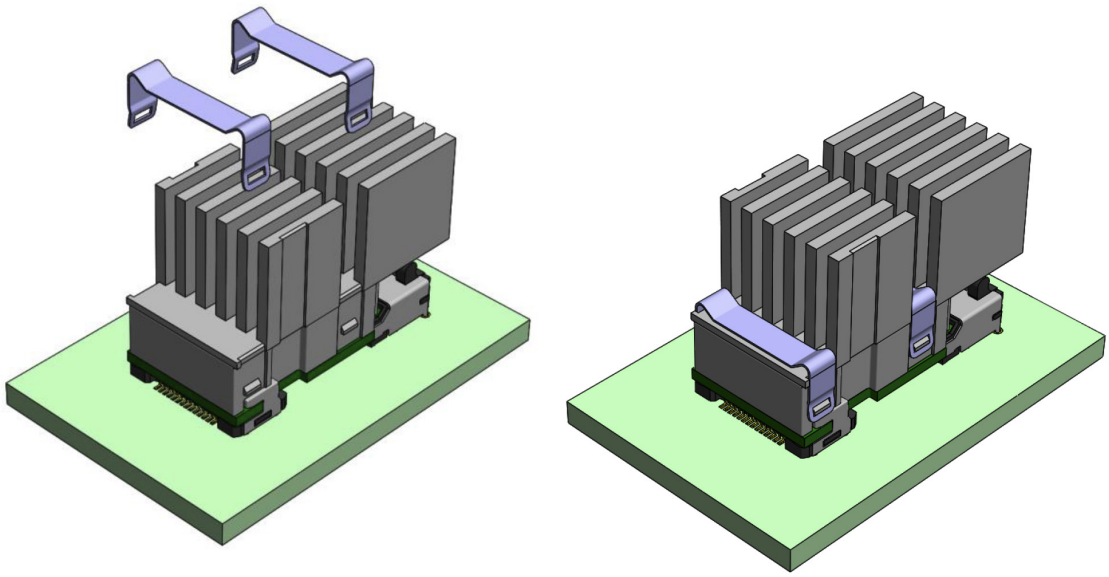


Figure 4-21: Heat Sink Attachment by Heat Spring Clip

The feature on the OBO that the heat sink clips latch onto requires a specific geometry on the spring clip to ensure robust and secure heat sink retention. Figure 4-22 shows the dimensions that must be implemented on the spring clip to ensure it latches securely to the OBO.

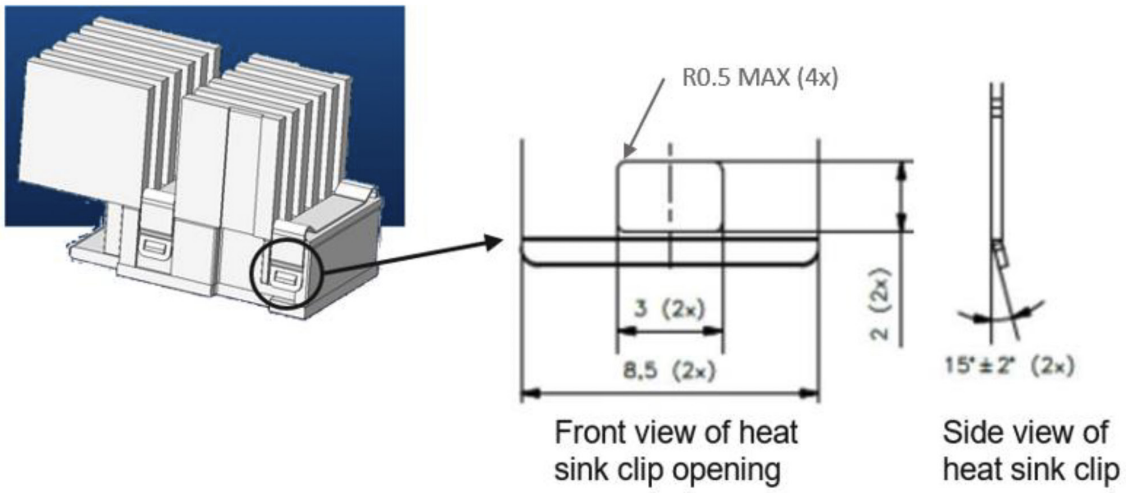


Figure 4-22: Heat Sink Clip

5.0 Environmental and Thermal

The equipment supplier is responsible for controlling the OBO case temperature to the specified range. The OBO supplier is responsible for defining a point on the OBO case where the temperature is measured. This should be a point connected to an internal component with the least thermal margin, e.g. a laser diode.

5.1 Thermal Requirements

The OBO case temperature may be within one or more of the case temperatures ranges defined in Table 5-1. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, utilizing the host systems designed airflow. For further information see Telcordia GR-63-CORE, Issue 4, April 2012, NEBSTM Requirements: Physical Protection.

Class	OBO Case Temperature
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

Table 5-1: Temperature Range Class of Operation

5.2 Thermal Requirements for Tighter Controlled Environments

The classes in Table 5-2 are intended for tighter controlled environments, e.g. data center environments as described in “Thermal guidelines for data processing environments”, fourth Ed., ASHRAE, 2015. The four classes correspond to different ranges of equipment intake air temperature.

Class	OBO Functional Case Temperature (Note 1)	OBO Performance Case Temperature (Note 1)
A1	15°C to 62°C	25°C to 62°C
A2	10°C to 65°C	20°C to 65°C
A3	5°C to 70°C	15°C to 70°C
A4	5°C to 75°C	15°C to 75°C

Table 5-2: Temperature Range Classes for Tighter Controlled Applications

Note 1: Functional includes all features available in low power mode. Performance means all specifications are met in high power mode.

6.0 Annex I: Power Supply Noise Measurement

6.1 Background

The pluggable module specifications for power supply noise referring to SFF-8431. This approach is adopted for OBO implementations and leverages:

- SFF-8431 A.1.1 normative noise generated from host power supply
- SFF-8431 A.1.2 normative noise fed back to the host power supply
- SFF-8431 A.1.3 normative noise tolerance from host to OBO module

6.2 Modifications to Method Specified in SFF-8431

The noise specifications and methodology remain the same other than the following changes to the power supply noise measurement method:

1. The filter is not prescriptive
2. The test point as close to the installed OBO as possible since neither the power supply nor the OBO is accessible for the compliant tests (see Figure 6-1). The measurement may be done on the other side of inter-connect which may be more accessible. If the measurement cannot be done at the LS connector; pad or pin, the lowest loop inductance point from the LS connector should be used for noise characterization. System implementers to measure the noise on Host board when the OBO's are installed

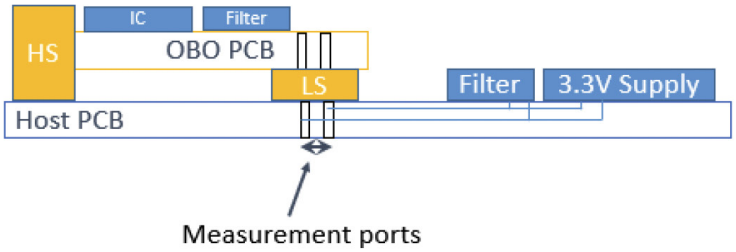


Figure 6-1: Power Supply Noise Measurement Location Example

3. Both the power supply noise and the EMI coupling would be examined
4. The suggested limit is 15mV rms

Consortium For On-Board Optics

COBO 8-Lane & 16-Lane On-Board Optics Specification

Release 1.1

For more information please contact info@onboardoptics.org